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Thin Films for Microelectronics and Photonics: Physics, Mechanics, Characterization, and Reliability[*]

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4.1. TERMINOLOGY AND SCOPE

4.1.1. Thin Films

Thin films of various types are a key component of modern microelectronic and photonic products. Conducting films form the interconnect layers in all chips, and dielectric films provide electrical insulation. With silicon-on-insulator (SOI) and strained silicon, semiconductor films have entered commercial design practice. The term *thin films* as used here refers to material layers deposited by vapor- or electrodeposition, with thicknesses too small to permit characterization by conventional mechanical testing procedures for bulk materials as described in, e.g., ASTM standards. Accordingly, our upper limit of thickness is taken as around 20 μm. Layers in this thickness range formed by other special processes, such as SOI (silicon on insulator) layers, also fall outside the standard mechanical test methods, and require thin-film characterization methods. Copper traces within multi-chip packages may be thicker than the definition given above, but some package designs include films within the present scope. Interconnect layers on die are included in a book on packaging because these layers are often considered to be "Level 0 packaging," since they are part of the packaging chain that connects the active devices to the outside environment electrically, mechanically, and thermally.

The relatively new field of microelectromechanical systems (MEMS) utilizes semiconductor fabrication techniques, especially lithographic patterning, to produce devices with moving parts and mechanical functions. Commercially important examples include

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accelerometers, used to trigger the deployment of automotive air bags, and pressure sensors. More recent examples are the movable mirrors used by Lucent, in optical switches, and by Texas Instruments, in Digital Light Processor (TM) systems. Thin films of a material set different from those in microelectronic devices are used for MEMS; polycrystalline silicon (polySi), designed for mechanical functions, is an important MEMS material.

The dimensions of films commonly used in microelectronic products have progressed well into the nanoscale at present, and MEMS technology is evolving the ability to produce nanoelectromechanical systems (NEMS). The elements of these products that are well below 1 μm in thickness challenge the current leading edge of mechanical characterization of thin films.

4.1.2. Motivation

The competitive pressure to produce "smaller, faster, cheaper" microelectronic devices means that reliability must be achieved using only the minimum amount of material, and also the minimum amount of testing. Actual testing of complete devices is the most definitive means to find out whether a design is reliable, and also the slowest and most expensive. Device designers use modeling and simulation to substitute for actual testing whenever possible. It seems evident that simulations based on an accurate understanding of the physics and mechanics of the materials involved, and carried out using accurate values of material properties, are more valuable than simulations based on *ad hoc* schemes and using guessed or estimated properties. The International SEMATECH roadmap has for years included the need for accurate modeling based on actual material properties. The 2003 version includes the statement [1]: *Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated.*

4.1.3. Chapter Outline

The current understanding of thin film materials has benefited from the energetic attention of materials science researchers. Several recent books discuss the deposition and behavior of thin films, with the general theme being the relationship between fabrication process, structure, and properties [2–5]. Since many different thin-film materials are critical components of various commercial products, and many different deposition processes are in use, this literature is voluminous. This chapter presents a broad overview of the physics and mechanics of thin films, with the goal of introducing topics and issues relevant to the reliability of films used in microelectronics and photonics. The latter sections, on mechanical properties and their characterization, treat their subjects in some depth. Again, however, complete descriptions must be sought in the original references. Section 4.2 presents a review of the physics and mechanics of thin films, with emphasis on basic physical features and recent findings relevant to the reliability of microelectronics and photonics. Section 4.3 introduces the physics underlying the most common failure modes and mechanisms of thin films, all of which relate closely to the state of stress, and argues that mechanical characterization is basic to design against these challenges; Section 4.4 reviews the techniques

available for mechanical characterization of thin films; Section 4.5 presents general expectations and rules of thumb for the mechanical behavior of thin films; and Section 4.6 gives results for some specific materials of interest for microelectronics and photonics. Section 4.7 identifies some issues where progress in understanding and characterization is urgently needed.

4.2. THIN FILM STRUCTURES AND MATERIALS

Microelectronic and photonic devices contain a variety of different types of thin films, introduced in this section. These devices are fabricated on massive substrates of single-crystal semiconductors. Millions, and more recently billions, of transistors must be placed on each die to create VLSI or ULSI (very or ultra large scale integrated) devices; semiconductor lasers and other photonic elements are also being driven to small form factors. A major branch of thin film technology, denoted as interconnect, has been developed to create the structures that connect these very tiny and unique active elements to each other and to the outside world. Interconnect films have thicknesses similar to metallurgical and anti-reflective coatings, but the deposition technologies and design schemes used in microelectronics and photonics are highly specialized. The reader should keep in mind that this book chapter focuses on films for microelectronics and photonics; information about the materials and deposition techniques particularly relevant to other technologies must be sought elsewhere.

Here we begin with substrates commonly used for electronic and photonic devices; we next touch on the conceptually simple but experimentally challenging case of epitaxial films; we introduce dielectric, metal, and polymer films, and special films for MEMS devices and for adhesion, barrier, buffer, and seed layers.

4.2.1. Substrates

The very idea of a thin film presumes the existence of a substrate; the difference in form and properties between film and substrate are fundamental to the state of stress in both the film and the substrate. Some useful values of mechanical properties of a few common substrate materials are given in Table 4.1. Crystalline substrate materials, especially silicon, are commonly elastically anisotropic, requiring three second-order elastic constants as shown in the table. Note that cubic symmetry is sufficient to ensure that the thermal expansion coefficient and the electrical and thermal conductivities are isotropic [6].

4.2.2. Epitaxial Films

An epitaxial film is a crystalline film on a crystalline substrate, where a lattice spacing of the film matches a periodic spacing of the substrate lattice. The benefit of epitaxy is that the microstructure of the film is controlled through selection of the substrate. Machlin gives a thorough, though "not encyclopedic", review of epitaxy [3]. He points out that many of the cases of epitaxy studied before 1985 were actually cases of graphoepitaxy. Examples would be metal films on sodium chloride or mica. These are cases of heteroepitaxy, because the film and substrate have different compositions. But graphoepitaxy refers specifically to the phenomenon where the bonding between the film and substrate atoms is so weak that the crystallographic alignment is produced by regular steps and terraces on the substrate

TABLE 4.1.

Selected room-temperature properties of some substrate and film materials [7–12]. Handbook properties are listed; microstructural effects such as texture may produce different values in specific cases.

Material	Crystal structure	Lattice parameter, Å	C_{11}, GPa	C_{12}, GPa	C_{44}, GPa	Aniso-tropy	Average Young's modulus, GPa	Average biaxial modulus, GPa	Biaxial modulus (100), GPa	Thermal expansion coefficient, $10^{-6}/°C$
Silicon	Diamond cubic	5.431	165.8	63.9	79.6	0.64	162.8	209.4	180.4	2.6
Germanium	Diamond cubic	5.658	128.5	48.3	66.8	0.60	131.6	166.0	140.5	5.8
Gallium arsenide	Zincblende (cubic)	5.653	118.8	53.7	59.4	0.55	116.2	153.1	123.9	5.74
Indium arsenide	Zincblende (cubic)	6.058	86.77	48.57	39.56	0.48	76.6	108.4	81.0	5.0[a]
Fused silica[b]	Amorphous	NA	NA	NA	NA	1	73.06	87.2	NA	0.49
Copper	FCC	3.615	168.4	121.4	75.4	0.31	128.2	195.4	114.7	16.8
Aluminum	FCC	4.050	106.8	60.7	28.2	0.82	70.0	107.3	98.4	23.6

[a] Average of values found in [10] and [11].

[b] The crystalline form of SiO_2 at room temperature is α-quartz. Its crystal structure is reported in the literature as both hexagonal and trigonal. It is actually trigonal, but is very close to hexagonal. Quartz crystals are used as a component in film thickness monitors in deposition systems. Ballato [13] notes an informative incident in the history of the measurement of the elastic constants of quartz. Atanasoff and Hart [14] made an extensive series of measurements of resonant frequencies of a set of quartz plates, as a means of measuring the elastic constants. Their worrisome conclusion was that their results were inconsistent with the trigonal symmetry then accepted for α-quartz. Later in the same year, Lawson [15] provided the explanation, that the piezoelectric nature of α-quartz influences its elastic behavior. By a proper mathematical consideration of the "converse piezoelectric effect," he showed that the experimental data of [14] were consistent with the trigonal symmetry, and provided a corrected set of elastic constants. These are listed in Table 4.1a. Table 4.1b lists the (hexagonal!) lattice parameters from [11] and thermal expansion coefficients for α-quartz from Touloukian et al.'s monumental work [12].

TABLE 4.1a.

Elastic constants of α-quartz, according to the trigonal crystal structure, derived by using the "converse piezoelectric effect" to correct the data of [14] at room temperature, from [15].

Elastic constant	Value, in units of GPa (or equivalently, 10^{10} dynes/cm^2)
C_{11}	86.75
C_{12}	6.87
C_{44}	57.86
C_{14}	17.96
C_{13}	11.3
C_{33}	106.8

To add yet another footnote to this cautionary tale, these same elastic constants are listed in [13], but C_{14} is shown with a different sign because [13] uses a different sign convention.

surface. Because graphoepitaxial films are prone to defects, they are not considered to be likely candidate materials for electronic or photonic devices.

Modern apparatus can maintain sufficiently high vacuum to produce true epitaxy, controlled by atomic bonding between the substrate atoms and the film atoms. The inter-

TABLE 4.1b.
Room-temperature lattice parameters [11] and thermal expansion coefficients
[12] for α-quartz, reported according to the hexagonal crystal structure.

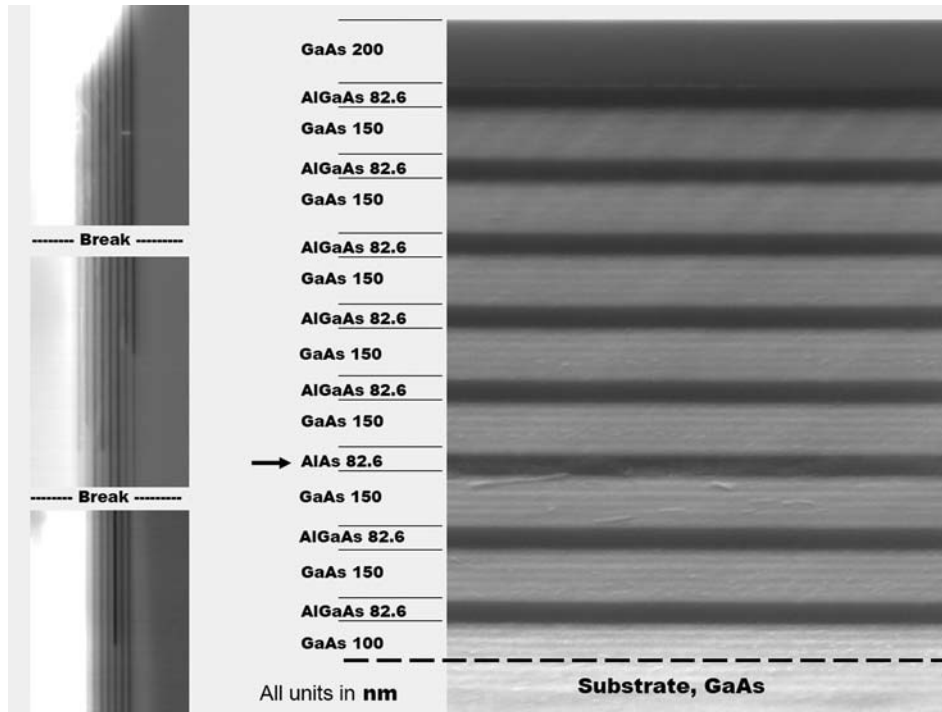| Direction	Lattice spacing, Å	Thermal expansion coefficient, 10^{-6}/°C
a	4.914	12.4
c	5.405	6.8

FIGURE 4.1. SEM micrograph showing heterogeneous epitaxial layers in a vertical cavity surface emitting laser (VCSEL) structure. This image is from a study of strains produced by oxidation of the AlAs layer [16,19].

face between epitaxial film and substrate can be more or less coherent, depending on the closeness of the match of their lattice parameters, the thickness of the epitaxial layer (or, epilayer), and other factors. According to Ohring [5], epitaxial deposition of silicon on silicon is the most commercially significant example of homoepitaxy, where the deposited material is of the same species as the substrate [5]. The epitaxial film is purer than the substrate and has fewer defects.

Technologically driven applications of heteroepitaxy are mainly in fabrication of optoelectronic devices made from wide-bandgap semiconductors. An experimental VCSEL (vertical cavity surface emitting laser) structure is shown in Figure 4.1 [16]. Intense commercial activity at present in this field has produced a bewildering variety of devices. Moglestue et al. describe the improvement produced by introducing AlGaAs layers into a GaAs photodetector [17]. The AlGaAs layers act as barriers to prevent the electrons and holes from traveling to low field regions in the GaAs; the result is improved perfor-

mance at high frequencies. Zirngibl et al. systematically describe a more sophisticated design [18]. These authors report a high-speed photodetector made of a strained superlattice of InGaAs/GaAs on a GaAs substrate. Here, the term "superlattice" refers to a series of alternating epitaxial layers of InGaAs and GaAs. In this example 120 pairs of layers were used, each on the order of 6 nm thick. The term "strained" refers to the fact that neither of the epilayers (epitaxial layers) fabricated in this study exists at its equilibrium lattice parameter, even though both the substrate and one of the layer types are composed of GaAs. This paper argues that the use of strained layers opens up the number of available materials systems for use in photonic devices, and that properly designed strained layers may remain stable and perform as well as lattice-matched layers. Epitaxy can be used to exploit even more sophisticated optoelectronic phenomena, such as distributed Bragg reflection and quantum wells and quantum dots.

The issue in all these structures is the manufacturability of a device with the needed electronic-photonic properties. The use of heterostructures may improve the optical performance, but may require that materials with different equilibrium lattice parameters be deposited in adjacent layers. The result is strain between the layers. If this strain becomes too large, the layer-to-layer interface will break down in some fashion, perhaps by the appearance of dislocations or other lattice defects, or perhaps by complete delamination. A thin layer can sometimes remain thermodynamically stable under more strain than a thick layer, because the strain energy accumulates with volume. But the variety of factors to be considered in selection of layer thicknesses includes a host of factors beyond strain, and may extend, for example, to the wavelength of light to be generated or detected.

So far we have considered only "blanket" layers covering the whole surface of a wafer. But designers are beginning to seriously consider quantum dot structures, where the epitaxy must extend in three dimensions, not just one. "Strain engineering" is the name of the effort to use strain effects to enhance the self-assembly and optoelectronic performance of quantum dots. Analytical techniques that treat the atoms in and around quantum dots are needed to fully describe their behavior; continuum mechanics calculations of strain provide only a rough estimate for the atomic displacements considered in the design of quantum dots.

4.2.3. Dielectric Films

It is often noted that the success of early thin film processes for metal-oxide-silicon (MOS) transistors was due as much to the robustness of readily produced silicon dioxide dielectric as to the semiconductor properties of silicon. One might also put the tenacious, electrically insulating natural oxide of aluminum into the list of material characteristics that contributed to the success of the aluminum–silicon dioxide interconnect structure. The traditional dielectric film for VLSI devices was some variant of silicon dioxide, for example, PECVD-TEOS, which stands for plasma enhanced chemical vapor deposition, using the precursor tetraethylorthosilicate. But for a variety of related reasons associated with electrical performance, which can be summarized as RC (resistive-capacitive) delay and power dissipation, insulating films with lower dielectric constant (k) are being incorporated into commercial devices [20]. These materials are known collectively as low-k dielectrics. The radical approach to the dielectric problem would be to use vacuum or gas as the dielectric, because vacuum has the lowest dielectric constant, and most gases do not raise it appreciably [21]. This approach has not yet proven to be popular but it is still being investigated. Silicate and silicate-carbonate films are the most widely studied and produced low-k films.
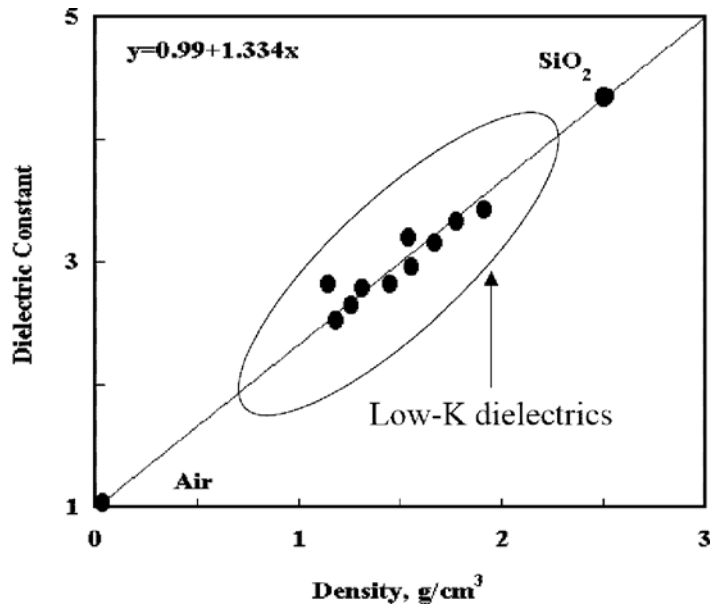
FIGURE 4.2. Dielectric constant plotted against density for a series of low-*k* dielectrics [25]. Values for air and SiO$_2$ are shown for reference.

These are amorphous materials and may be made highly porous to further reduce the dielectric constant. Figure 4.2 shows the trend for dielectric constant with density. This trend raises a problem, because the decrease in density implies an increase in porosity. Most low-*k* materials studied so far lack mechanical strength; the strength tends to go down along with the dielectric constant [22], because the lower-*k* materials are more porous. Volinsky et al. used nanoindentation, discussed below, to document the mechanical weakness of some low-*k* films [23–25]. The lack of strength is an issue because the interconnect stack on the back of a ULSI device is built up layer by layer, so that the first layers must be able to survive the manufacturing steps applied to later layers, especially CMP (chemical-mechanical planarization). The move to flip-chip designs, with solder bumps placed on top of the interconnect stack, means that the interconnect stack requires a certain degree of mechanical robustness. An improved low-*k* material would aid both manufacturing yield and device performance, so there is a great deal of research under way in this field at present.

4.2.4. Metal Films

Metal films are used in interconnect structures for their electrical conductivity. In the last few years, copper has displaced aluminum from ULSI devices largely because of its higher conductivity, even though it lacks the robust natural insulating oxide of aluminum. Highly reflective metal coatings are key elements in optical switch structures. Adhesion of the film to the substrate is important for useful films. Careful polishing, etching, and cleaning techniques are applied to commercially available substrates. The cleanliness of the substrate and the deposition system is critical to adhesion. A typical practical film deposition process for a metal film such as aluminum or copper onto a silicon substrate might include plasma cleaning of the substrate within the deposition chamber and the use of an adhesion layer such as Ti or Ta. A film intended for use as a conductor might have a thick-

ness around 1 μm, although large variations, say from 0.1 to 10 μm, are found depending on what the purpose of the film is and where it is located in the interconnect stack. In electrodeposition, the adhesion issue applies to both the seed layer on the substrate and the electrodeposit on the seed layer. The purity of the electroplating solution is obviously important.

4.2.5. Organic and Polymer Films

Organic polymers are traditional insulators used with metallic conductors and as coatings on optical fibers. Two examples are benzocyclobutene (BCB) and polyimide (PI). These polymers feature good thermal and mechanical stability; some varieties are photo-sensitive, which adds processing efficiency. These materials have elastic moduli only a few percent of those of metals, so they are highly compliant. Their strength can be comparable to that of metal films, ranging up to 100 MPa.

Organic semiconductors are being considered as active electronic elements for price-sensitive applications, where ULSI integration and gigahertz performance are not required [26]. Early organic semiconductor transistors were primitive [27], but considerable progress has been made since then. Organic semiconductors still face a challenging set of obstacles before widespread commercialization [28]. In particular, their reliability is likely to be an issue; few standard mechanical characterizations of such materials have been reported.

4.2.6. MEMS Structures

Microelectromechanical systems are microscopic mechanical systems constructed by use of the powerful photolithographic techniques developed in the microelectronics industry. Controllable micromirror arrays, accelerometers and orifices for inkjet printing are the leading commercial applications of MEMS at present. The fabrication of MEMS relies on chemical etching to remove one or more sacrificial layers. Typical materials used are a silicon nitride film to passivate the silicon substrate, followed by alternating layers of BSG (borosilicate glass, the sacrificial layer), and polySi. After the sacrificial BSG layers have been removed, the polySi mechanical elements become free to flex, extend, or rotate. MEMS-style structural elements, such as cantilever beams, are sometimes used as mechanical test structures for non-MEMS materials systems such as CMOS, as well as for MEMS materials [29]. The polySi layers are deposited by a chemical vapor deposition (CVD) route. The grain sizes of some very strong and adherent polySi films are quite small, only a few nanometers, and the strength may approach the traditionally predicted strength limit for crystalline solids, around one-thirtieth of the Young's modulus [30].

The packaging of MEMS systems is often very challenging and expensive, especially when the device must be in contact with the external environment. MEMS-style lithography techniques have been used to fabricate microfluidic devices, the "lab on a chip," which may become powerful tools for chemical analysis and bioassays.

4.2.7. Intermediate Layers: Adhesion, Barrier, Buffer, and Seed Layers

The use of one or more intermediate layers is a time-tested strategy in the design of thin film structures. The thickness of such layers is typically thin compared to the layer they are included to promote, and their electrical properties may be poor or irrelevant. A classic

example of buffer layers for chemical stability is the under bump metallurgy (UBM), the series of layers between the top ULSI interconnect layer and the solder. The need for intermediate layers, such as nickel, between aluminum and solder is evident, because to this day aluminum can be soldered only with great difficulty. However UBM is still considered useful for chips with copper interconnect layers [31]. Probably the earliest example of intermediate layers is the use of chromium below gold films on glass or quartz, to dramatically improve the adhesion. While both titanium and chromium [32] promote the adhesion of copper to SiO_2, titanium, tantalum (tantalum nitride), and Ti-W are more likely to be found in ULSI devices.

In today's competitive microelectronics/photonics design environment, the mantra "smaller, faster, cheaper" may also imply hotter, because higher operating currents promote speed. An important deleterious effect of higher temperatures on integrated microelectronic devices may be due to enhanced diffusion of chemical species into, out of, or through thin films. This issue was encountered in the silicon–aluminum–silicon oxide system when silicon diffused into the aluminum, causing a variety of problems. These were mitigated by alloying the aluminum films with a small amount of silicon, to prevent the uptake of additional silicon by the films. Later, when aluminum films containing a small amount of copper came into use because of their better electromigration resistance, titanium and titanium nitride barrier layers were used. This problem has grown more severe with the copper–silicon systems, and is controlled by the use of barrier layers to prevent copper from diffusing into the surrounding dielectric [33,34]. Titanium nitride and tantalum nitride barrier layers are used. A barrier layer that also enhances adhesion is clearly a design efficiency, and both titanium and tantalum nitride layers promote adhesion as well as serving as diffusion barriers.

It was noted above that coherent epitaxy and minimization of strain are incompatible objectives for heteroepitaxy when the epi layer has a lattice parameter different from that of the substrate. Buffer layers are used to "spread out" the strain. In such a case, the intermediate layers would be alloy layers sharing the composition of the substrate and epitaxial layers, with a graded composition to grade the lattice parameter.

Electrodeposition requires a conductive seed layer that is electrochemically compatible with the plated layer. The most straightforward choice is to use a seed layer of the same chemical element as the plated layer, for example, a copper seed layer for copper electrodeposition. The seed layer, of course, must be deposited by some technique other than electrodeposition, especially when the substrate is insulating. While copper seed layers have been used for ULSI designs with copper interconnects, research is in progress to use the barrier layer as the seed layer [35]. A combination seed, barrier, and adhesion layer would be an admirable example of design efficiency. As yet the verdict is still out on the ruthenium-copper system for ULSI.

4.3. MANUFACTURABILITY/RELIABILITY CHALLENGES

Manufacturability and reliability are critical when failure of a single transistor among millions can negate the economic value of a die. Producers of films for electronics and photonics are invariably most concerned with functional diagnostics; for example, does the film meet its intended electrical or optical performance criterion, such as electrical resistivity or optical reflectivity? But functional failures have their roots in the physical and mechanical behavior of the films. The selection of topics for this chapter has been guided

toward those relevant to manufacturability and reliability of microelectronic and photonic devices.

We note that mechanical failure is not the only threat to electronic devices; electromigration is included here as a special case because it clearly falls under the topic of reliability and it is a thin film failure mode. The prevention of corrosion, whether electrochemical or not, is an important necessity in the design and manufacture of electronic devices. But for corrosion, the physics and mechanics of thin films are secondary to chemistry, so it is left to the reader to pursue this topic elsewhere.

Throughout thin film technology, the concept of stress has been utilized as a guide to understanding, predicting and preventing instances of mechanical failure. Stresses created in the film deposition process are measured and minimized; sources of stress during service are identified and controlled; the response of materials to stress, namely, mechanical properties, are characterized and optimized; and even quantities that may influence the response of a thin film to stress, such as grain size, are considered and monitored.

4.3.1. Film Deposition and Stress

4.3.1.1. Thin Film Deposition Processes   A set of deposition processes used for crystalline materials such as metals and ceramics applies energy to the film source material to separate individual atoms from the source and to launch them toward the substrate. Outlines of the principles of some methods for film deposition are given here to introduce the basis of some of the manufacturability and reliability issues; a complete treatment can be found in [4]. In *physical vapor deposition (PVD)*, commonly used to produce metal films, thermal energy is supplied to the source material by heating it, either electrically or by a directed electron beam. As the source material approaches its boiling temperature, individual atoms fly off the surface and travel in random directions. The process is carried out in vacuum, so that the atoms can reach the substrate before colliding with atmospheric gases. The usual practice is that only the source itself is hot, so the atoms are deposited on whatever surface they encounter first, which is often, but inefficiently, the walls of the vacuum chamber. The rate of production of free atoms is expressed in plots of vapor pressure *vs* temperature. The residual pressure in the deposition system, the composition of the residual gases, the temperature of the source, which controls the rate of evaporation, the temperature of the substrate, the distance from source to substrate, and the duration of the deposition are important variables. In *sputtering*, the source is bombarded with energetic atoms, usually atoms of an inert gas such as argon. Atoms from the source are knocked or "sputtered" off the surface, and travel around the chamber, sometimes steered by electric or magnetic fields. The pressure and energy of the sputtering gas are important parameters specific to this process. An advantage of sputtering is that source materials with low vapor pressure at practical temperatures can be deposited. The stress in sputtered films is highly variable, depending on the deposition conditions. Epitaxial films were discussed above; in *expitaxial* deposition, the uniformity of the crystal structure of the substrate surface, a carefully chosen match between the crystal structures of the substrate and the deposit, and overall cleanliness are the key issues. In *chemical vapor deposition*, the source is not used in pure form, but rather in the form of a chemical compound that can be transported into the deposition zone as a vapor. Within the deposition zone, a chemical reaction occurs, typically controlled by heating the substrate, which converts the element to be deposited to a form that sticks to the substrate and forms a solid film. Since the source is gaseous, it can be prevented from sticking to the walls of the deposition chamber or to any surface

it encounters by controlling their temperatures; therefore complex and highly curved surfaces can be coated. In *electrodeposition*, the electrically conductive source material and the substrate are immersed in a plating solution. Individual atoms or clusters of atoms are separated from the source by a combination of chemical dissolution and the local electric fields at the surface. The electric field set up between the substrate and the source directs the dissolved atoms to the substrate, where the local electric field promotes their incorporation into the deposit. This process incorporates a host of new variables, including the chemistry and temperature of the solution, the voltage, and the current density. An important consideration is the seed layer, needed to establish the electric field before any plating occurs. Additives or impurities in low concentration in the plating solution can influence the plating process significantly. Polymer films, which are rarely crystalline, are deposited by spreading a thin liquid layer of polymer, often mixed with solvent, on the substrate surface and drying and baking it. Typical examples are photoresist and polyimide.

In all deposition process, atoms collect on the substrate in structures that initially have low density and low order compared to the equilibrium structure of the film material. The mechanisms by which crystallographic order is gradually recreated within the deposited film have been subjects of intense study, as reviewed by Machlin [3] and other investigators cited therein. A key feature of these processes is the creation of stress in the newly deposited film.

4.3.1.2. Thin Film Stress   It is safe to say that stress occurs during every thin film deposition process, although specially designed processes may be capable of eliminating stress, for example, by the incorporation of high temperature annealing built into the process. As an atom of the species being deposited strikes the substrate it loses most of its kinetic energy, especially if the substrate is maintained at a temperature well below the melting point of the film material. Stresses arise when the deposited atoms lack sufficient thermal energy to diffuse far enough and long enough to assume their equilibrium conditions of density and crystal structure. Stresses remaining after the substrate and film reach room temperature are termed "intrinsic" stresses; some authors use the term "residual stresses." Doerner and Nix have reviewed several stress-generation mechanisms [36]. Detailed schemes relating the deposition temperature to the stress are given in [3]. Floro et al. discuss the evolution of stress in SiGe and selected metals [37]. Sputtering is capable of producing compressive stresses. Deposition stresses may be great enough to peel a film from the substrate, to create plastic strains through stress relaxation, or to distort the shape of the substrate, creating the infamous "potato chip" effect. Ohring [5] gives a table of stresses encountered in several films, mainly dielectrics, but notes that the stresses are highly dependent on experimental variables and that no quantitative predictive theory is available.

At this point it is worth considering just what is meant by the phrase "thin film stress." Conceptually, as with stress in a small volume element of a continuum, the existence of stress implies that the atoms in the stressed element are constrained in a state of elevated elastic potential energy, which relieves itself instantaneously when the element is freed to deform. Four types of stress are traditionally distinguished: externally applied; lattice misfit; intrinsic, as defined above; and thermal. Lattice misfit stresses were mentioned above in the context of epitaxy. The principle is that the epitaxial layer may have an equilibrium lattice parameter different from that of its substrate; the rigid substrate prevents the epitaxial layer from stretching or shrinking to reach its nominal lattice parameter; thus, the epitaxial layer is in a state of stress. Thermal stresses arise when two materials with different thermal expansion coefficients are joined, and then heated or cooled while held rigidly in place. There are three main operational definitions or "acid tests" for the presence of film stress:

(a) if a substrate deforms evidently during a deposition process, or if a film spontaneously peels from a substrate, as described in the previous paragraph, one deduces that the film was stressed so highly that its tendency to deform could not be resisted by the substrate or by the adhesion of film to substrate; (b) if one of the crystal lattice parameters of the film is found to be different from its value in the bulk, stress is suspected, because films thicker than a few atomic layers have the same equilibrium lattice parameters as the bulk; (c) if a film is deposited on a previously flat rigid substrate, and the substrate is subsequently found to be curved, one deduces that stress in the film is the source of the force needed to elastically deform the substrate. Measurements of film lattice parameters, by X-ray techniques, and of substrate curvature, mainly by optical techniques, are discussed next. It is also noted that Swadener et al. have reported that intrinsic stress can be measured using depth-sensing indentation [38]. As discussed below, nanoindentation can also promote observable delamination of film from substrate; this phenomenon can be used as a diagnostic for film stress.

X-ray methods are common for measurement of lattice parameter and crystallographic texture for metal and ceramic films of all types. They can even provide some information about amorphous films in special cases. Grazing incidence X-ray reflectometry can be used to measure the thickness and density of very thin layers; the upper limit is poorly defined but is of the order of 0.1 μm. Gravimetric methods of measuring film density are impractical. Many characterization techniques applied to films, such as for example electrical conductivity or sound wave speed, depend on both the thickness and the density. The density is typically assumed to be nominal, but this is not necessarily the case. Therefore, X-ray reflectometry methods, even though they require special apparatus, may be advantageous in some cases because of their specificity.

X-ray diffraction to characterize a thin film can be carried out using a diffractometer set up for measurements of "powder patterns," with an appropriate specimen holder. The incident radiation would have a monochromatic spectrum. For a typical metal film deposited under relatively normal conditions, the X-ray diffraction record reveals the same crystal structure as for the bulk material; for example, the face-centered-cubic (FCC) structure of aluminum, copper, and gold is maintained. The diffraction peaks would be broadened, relative to bulk materials, due to the smaller thickness, grains, and subgrain domains in thin films. The intensity is low because the scattering material is only about 1 μm thick, but it is sufficient even for general-purpose instruments. The spectrum might be interrupted if a strongly-scattering set of planes in the substrate comes into alignment with the X-ray source and detector. In films just as in some bulk metals such as drawn wires or rolled plates, the relative amplitudes of the peaks may be influenced by preferred orientation or texture of the film. Measurements over a wide range of solid angles are needed to accurately evaluate the film texture. The lattice parameters deduced from the spectrum give essentially the same values of lattice parameter as listed in the handbooks for bulk material of the same composition. X-ray diffraction can be used to evaluate intrinsic stress if the lattice parameter can be measured with sufficient accuracy, and if, importantly, the value of the lattice parameter of the film material in its unstressed condition is known. However, most of the literature reports on this approach are for hard films rather than electronic interconnect materials.

Curvature measurement techniques for both wafers and cantilevers have been used to follow stress evolution, e.g., [37,39]. Wafer curvature as applied to mechanical properties measurement will appear again below. However, we note that Malhotra et al. [40] reported a difference between stress measured by curvature and by X-ray diffraction. The Stoney formula, which relates substrate curvature to film thickness and stress, contains the biaxial

elastic modulus. Because of the power of this equation in a variety of measurement and application contexts, it will be described below. Example data sets needed for application of this equation were given in Table 4.1. The concepts of tensor elasticity are used to relate single crystal elastic moduli, in particular the stiffnesses C_{ij} or the compliances S_{ij}, to practical moduli such as the biaxial modulus in the substrate plane [2]. Representative elastic moduli of polycrystalline aggregates are relevant for metal films like aluminum and copper. Some useful examples were listed in Table 4.1. de Lima et al. studied the thermal expansion coefficients and biaxial moduli for several combinations of materials relevant to microelectronics and photonics [41]. The scatter among their data and differences between their thin-film data and bulk values indicate that both preparation of representative specimens and carrying out precise and accurate measurements of these properties remain experimental challenges.

The Stoney formula is

$$\sigma_f = \frac{M_s t_s^2}{6R t_f}.$$
(4.1)

Derivations, and the link back to the original source of this formula, are given in [2] and [5]. Here σ_f is the stress in the film; M_s is the biaxial modulus, given by $M_s = E_s/(1 - \nu_s)$, where E_s is the Young's modulus of the substrate and ν_s is the Poisson's ratio of the substrate; t_s is the thickness of the substrate; t_f is the thickness of the film, and R is the radius of curvature of the substrate. This equation shows that for no curvature, where R is infinite, the stress in the film is zero. As the curvature increases, R becomes finite and the stress increases. For a given curvature, the stiffer the substrate (high M_s value), the larger the stress. And, for a given curvature, the thicker the film, the smaller the stress. This formula as written assumes that the stiffness of the thin film is negligible compared to that of the thick substrate. The assumption implies that Equation (4.1) can be applied without knowledge of the elastic properties of the film, an advantage in some cases.

The Stoney formula can be extended to a 2D case:

$$\sigma_R = \frac{E_s}{1 - \nu_s} \frac{h_s^2}{6h_f R_1} \left[1 + \left(\frac{\nu}{1 + \nu} \right) \cdot \left(\frac{R_1}{R_2} - 1 \right) \right],$$
(4.2)

where R_1 and R_2 are the radii of curvature in the x–z and y–z planes respectively.

Substrate curvature radii can be measured accurately with laser deflection and optical lever cantilever beam techniques. This allows constructing a stress map over the whole wafer (Figure 4.3). Recently Shen et al. [42] have extended the curvature methods to measure residual stresses in patterned line structures. Treatment of MEMS-style cantilever beams, where the thicknesses of the two layers are comparable, would require a more complete formulation.

4.3.2. Grain Structure and Texture

A second major consequence of film deposition processes is that thin films generally are polycrystalline with grain sizes much smaller than bulk materials. Epitaxial semiconductor films are an exception, of course, and polymer films have no grains, hence no grain size. Relevant examples are all metal films produced by physical vapor deposition (PVD) or electrodeposition. Polycrystalline silicon (polySi) is not known in bulk form, but CVD
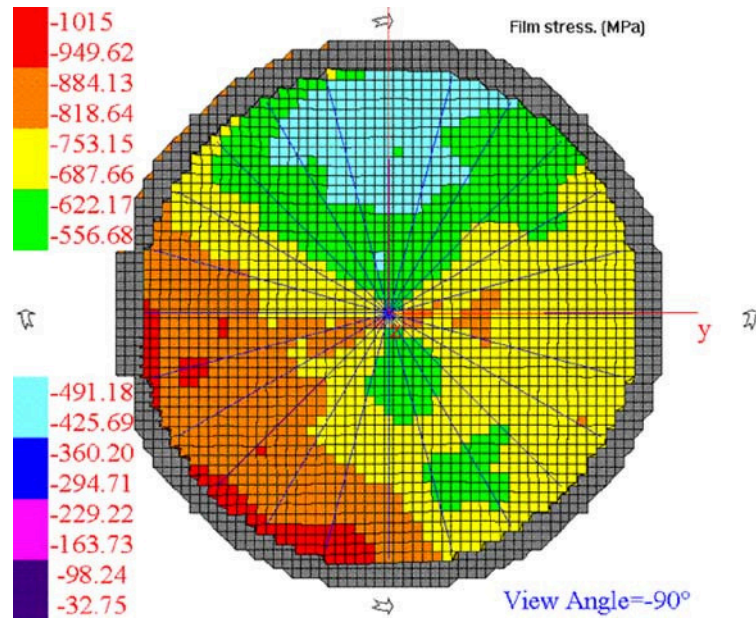
FIGURE 4.3. Residual stress map of a TiW_xN_y film 1 μm thick on a 150 mm diameter GaAs wafer.

polySi films have a very small grain size, well below 1 μm. Grain sizes of 1 μm in PVD metal films are commonplace; the effects on strength will be discussed below. In fine-grained films the volume of material in and near grain boundaries has been considered to be large enough to influence the overall behavior of the film, including density and elastic properties. Machlin [3] gives an extended treatment of the structure zone model, which relates the grain structure to the film growth conditions, particularly the substrate tempera-ture. Figure 4.4, from [43], presents an overview that applies to metal films.

It is important to measure thin film grain size, since it affects the mechanical proper-ties, specifically yield stress. Grain boundary scattering of electrons in very fine metal lines is now considered to have a serious deleterious effect on the electrical conductivity [44]. In the case of a nanocrystalline columnar grain Cu film, the in-plane grain size can be measured by means of atomic force microscopy (AFM), where grains can be resolved on the surface. The out of plane grain size is typically equal to the film thickness for films with thickness of a few hundred nanometers. Measurements from the AFM section analy-sis provide the average grain size. One of the problems with measurements of grain size of electroplated Cu films is that annealing causes grain coalescence through the film thickness, but not necessarily surface reconstruction that would replicate the new bigger grain size. Focused ion beam imaging (FIB) is a more suitable technique than AFM for thin film grain size measurement, because it directly samples the lattice, not the surface topography. It is similar to scanning electron microscopy (SEM), but instead of the electron beam, a focused ion beam of gallium is used to raster along the sample surface. The image is constructed by collecting secondary ions or electrons, which produce a contrast according to the grain orientation. The FIB can also be used to clean oxide from the surface by sputtering. A FIB image of a 2 μm thick electroplated Cu film is displayed in Figure 4.5. The sample is tilted 45° to the ion beam, so all grains appear elongated in the horizontal direction. Grain size can be directly measured from such an image, where much of the intragranular contrast
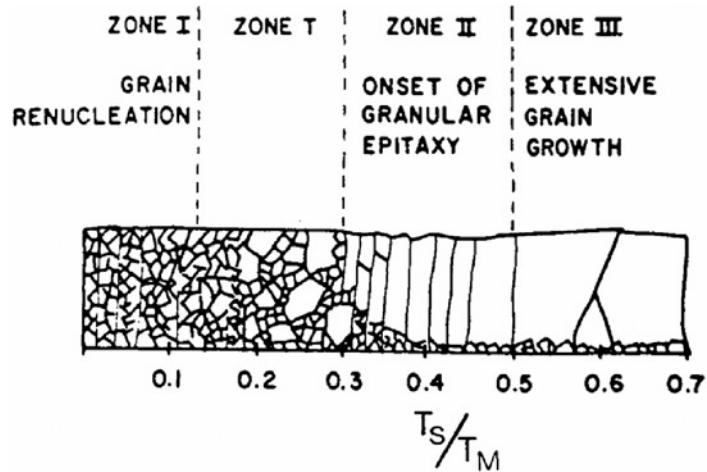
FIGURE 4.4. Effect of substrate temperature on the grain structure of a metal film. T_s/T_m is the ratio of the substrate temperature to the melting temperature of the film material in bulk form [43]. Figure reprinted with permission.
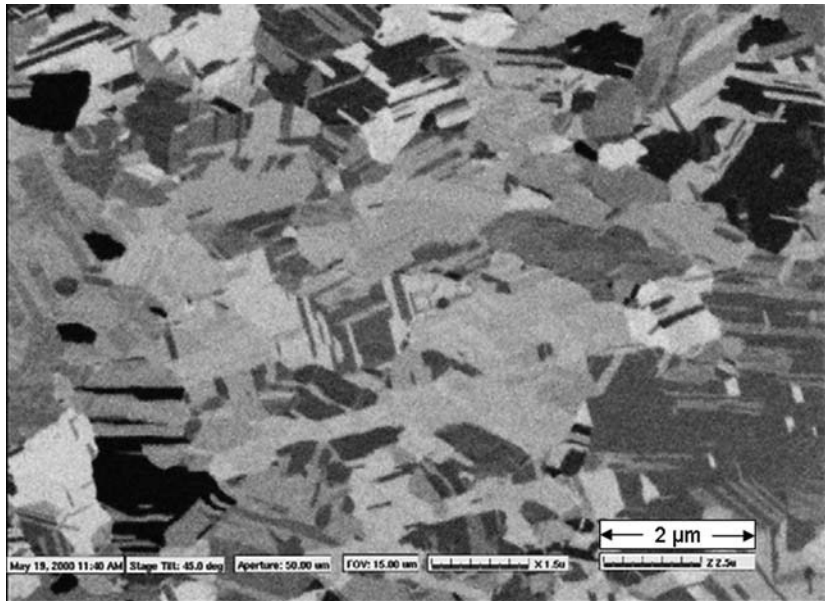

FIGURE 4.5. Focused ion beam image of a 2 μm thick electroplated Cu film (45° tilt).

is due to Cu twinning. While more time consuming, especially because of the specimen preparation required, TEM is the definitive technique for grain size measurements. The new SEM technique of electron back scatter diffraction (EBSD), combined with precise cameras and special software, is a powerful technique for crystallographic measurements in films with clean, flat surfaces.

Crystallographic texture is the third property that arises as a result of the deposition process. X-ray diffraction is the technique typically used to measure thin film texture; the
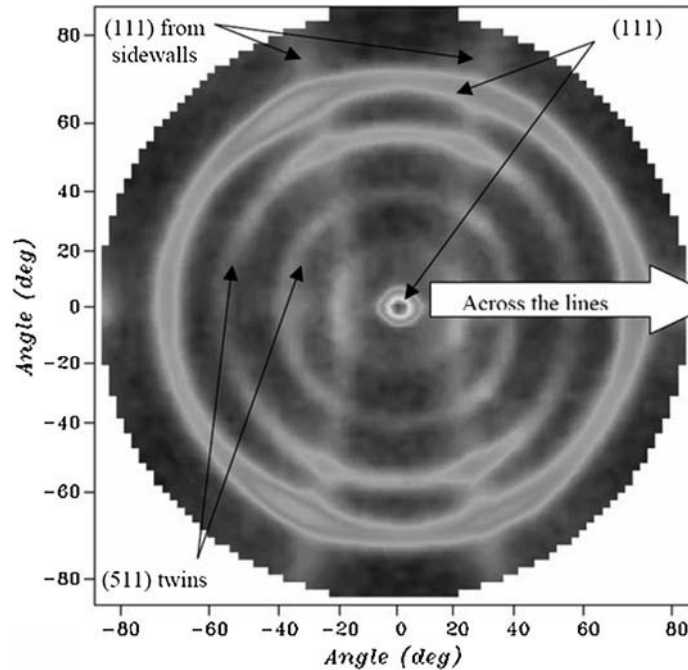
FIGURE 4.6. (111) pole figure of a 500 × 500 μm array of parallel Cu lines on a TaN underlayer. The direction transverse to the lines is indicated. The (111) fiber texture of the film on the wafer surface and the (511) twins appear as the central spot and the rings, indicated by arrows in the image. The sidewalls of the damascene lines produce (111) reflections that form the curved bands from top to bottom.

theory for the measurements is adopted from treatment of bulk materials [45]. In blanket films as-deposited in typical processes, the only special direction is the direction perpendicular to the substrate, especially since substrates are often rotated during deposition to ensure that the film properties are the same along all in-plane directions. The resulting thin-film textures are fiber textures, symmetrical about the direction perpendicular to the substrate. Aluminum films made by PVD commonly have a strong (111) texture. Typically electroplated Cu films have (111) texture, sometimes with a weak (100) component. Some film patterning process, such as lift-off and damascene, deposit metal on a patterned substrate; these patterns can introduce their own characteristic crystallographic texture. Even though the residual stress and the mechanical properties of various Cu films are very similar, the X-ray pole figure analysis technique can show the difference in electroplated Cu films on different underlayers in terms of their microstructure. Figure 4.6 shows a (111) pole figure obtained from a horizontal array of Cu interconnect lines on top of a TaN underlayer. The pole figure shows standard (111) peak intensities at 0 and 70.5°, as well as (511) twins. The fainter vertical features are the (111) intensities from the interconnect sidewalls. Electron back scatter diffraction can be used to evaluate texture, as well as grain size, because the diffraction patterns can conveniently be analyzed to give the complete crystallographic orientation of the sampled volume of material.

The crystallographic texture of electrodeposited copper films can change with time for hours or days after deposition [46]; silver appears to share this behavior. This texture evolution is just one among several manifestations of the change in microstructure of elec-

trodeposited copper films that can occur at room temperature—certain grains can also grow by recrystallization. Annealing accelerates the effects.

Zhang et al. [44] report a careful study of the electrical resistivity of electrodeposited copper. They conclude that the effects of grain boundaries are significant in raising the electrical resistivity of their films. For relatively thick films, they report a combined resistivity effect of 0.08 microohm·cm for impurities and grain boundaries. This is lower than a value reported over 10 years earlier for PVD films, discussed below. This study [44] is relevant to a current "hot topic," the increase of electrical resistivity with decreasing film thickness. Zhang et al. observe the resistivity increase with decreasing thickness, but attribute the greater part of the effect to the smaller grain sizes in the thinner films. The effect of line width on electrical resistivity was discussed by Hanaoka et al. [47] and by Josell et al. [48].

The physics behind these resistivity phenomena is based on the electron mean free path. The mean free path in pure bulk copper at room temperature is limited by electron-phonon scattering. The existence and significance of electron-phonon scattering can be evaluated from measurements of resistivity as a function of temperature. As the temperature is lowered, the phonon density decreases, the mean free path increases, and the resistivity decreases dramatically, especially in very pure materials. The residual resistivity ratio (RRR), which is the resistivity at room temperature divided by the resistivity at 4 K ($-269°C$), can reach values in the thousands for bulk specimens of very pure copper. Values of the RRR for thin films are much lower.

As linewidths reach the room-temperature electron mean free path in copper, the effective resistivity increases because electrons scatter from the sidewalls, top, and bottom of the line. However, electrons can scatter in different ways. Diffuse scattering, where the final velocity is randomly distributed, has a large effect, whereas specular scattering, where the electron retains its momentum in the plane of the boundary, has no effect. So a need for control of the roughness of the edges of narrow interconnect lines (line edge roughness) has been hypothesized; however experimental achievement of surfaces smooth enough to reduce diffuse scattering of electrons has not been reported. This effect is taken seriously, to the extent that novel alternatives to copper are being actively discussed, such as carbon nanotubes, which may offer "ballistic conduction," where the electron flies unimpeded down the bore of the nanotube.

4.3.3. Impurities

The rain of metal atoms impinging on and sticking to a substrate during film deposition as described above in Section 4.3.1.1 is accompanied by a rain of impurity gases, even in PVD systems with very good vacuum. Some of the gas atoms remain in the films. Similarly, impurities from an electrodeposition solution are deposited along with the intended metal. These components may be deleterious to the electrical conductivity of a film, but they are generally carefully controlled only during epitaxial growth of multilayer semiconductor films.

The best current value for the electrical resistivity of pure bulk copper at room temperature (300 K) was given by Schuster et al. as 1.72 microohm·cm [49]. These authors also give a detailed discussion of the temperature dependence of the resistivity of copper. Johnson [50] studied the electrical resistivity of copper and nickel thin films produced by thermal evaporation under a range of deposition conditions relevant to electronic interconnects. He noted that an impurity concentration of around 1% was typical for his PVD films; this produced a resistivity increase of about 0.2 microohm·cm. Johnson examined other possible sources of electrical resistivity in his thin films and concluded that

the next largest contribution, about 0.1 microohm cm, was from intragranular dislocations (discussed below), and that the contributions of the remaining possible sources were insignificant. Johnson concluded that PVD copper films made under optimized deposition conditions can be expected to have electrical resistivities 18% higher than the bulk copper value. He found the situation for nickel to be different in some aspects, with a much worse achievable electrical resistivity.

4.3.4. Dislocations

A dislocation is a line defect in a crystal lattice [51], familiar from undergraduate materials science. Dislocations are a concern in all the crystalline materials in electronic devices. Silicon wafers are carefully handled to make sure they are practically "dislocation free," because dislocations would offer paths for current leakage and fast diffusion, as well as likely sites for impurities. The effects of dislocations in other crystalline substrates are similarly undesirable. Dislocations may play a slightly more constructive role as strain-absorbing structures at sites of lattice-parameter mismatch, for example, in heteroepitaxy or around quantum dots. The intentional use of dislocations in such structures is in its infancy at present, and its future is uncertain. The typical approach today is to seek to control creation of dislocations through the use of graded buffer layers.

Metal films made by PVD contain a large dislocation density compared to familiar bulk materials. This is an issue because dislocations, along with surfaces and grain boundaries, raise the electrical resistivity and are paths for rapid diffusion. Dislocations exacerbate the failure modes of diffusion, which can create unwanted conduction paths, and electromigration, which can cause open circuits. Figure 4.7 [52] shows dislocations in an
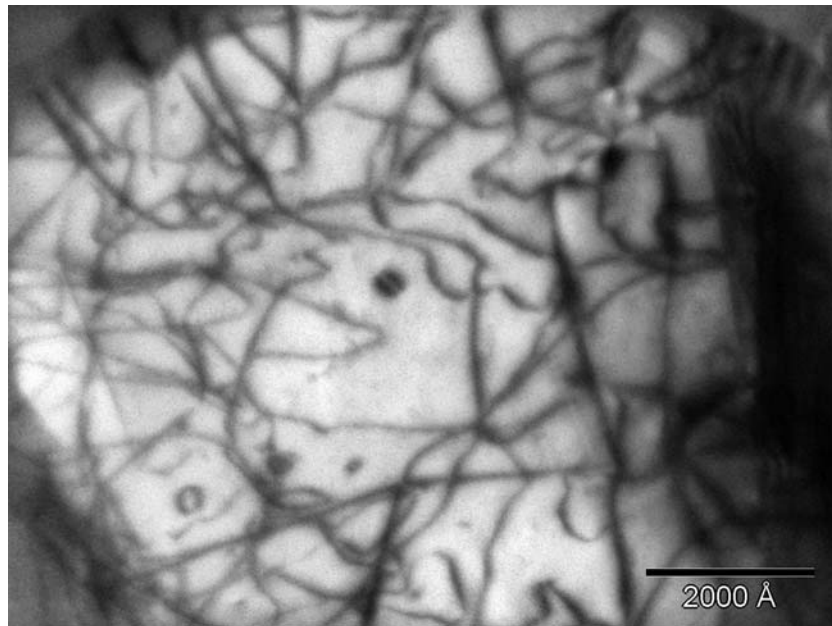

FIGURE 4.7. TEM micrograph of a thin film of aluminum, as grown. The dark lines are dislocations, which produce contrast because the crystal lattice is disturbed at the dislocation core. The dislocation density is about 2×10^9 cm^{-2}.
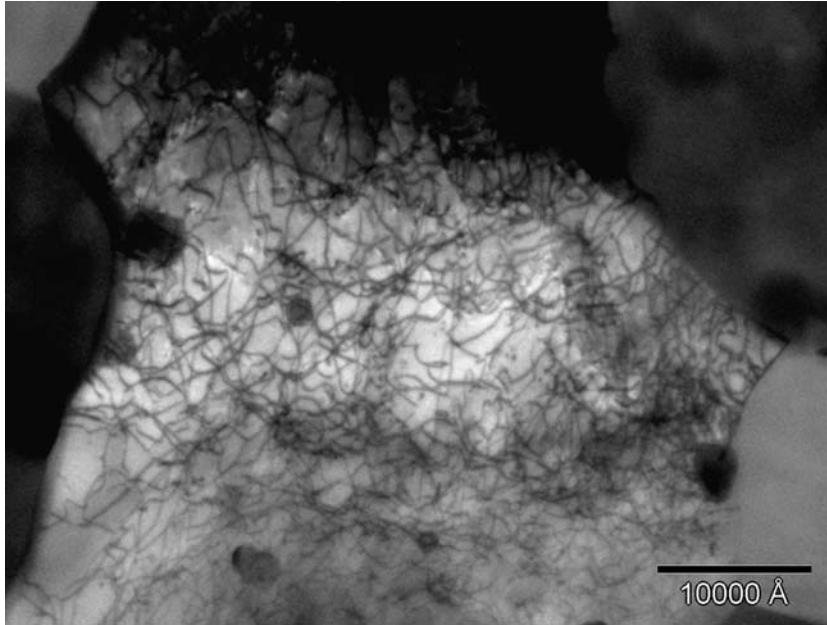
FIGURE 4.8. TEM micrograph of a thin film of microtensile specimen of aluminum, strained to failure in tension. The dark lines are dislocations. The dislocation density is about 10^{11} cm^{-2}.

aluminum film deposited as contact metal in a commercial CMOS process. The dislocation line density is about 2×10^9 cm/cm^3. Dislocations were discovered as the mechanism for plastic strain in metals, and mobile dislocations are the carriers of plastic strain in sufficiently thick metal films, as can be discovered by TEM examination of microtensile and nanoindentation specimens. Figure 4.8 [52] shows dislocations in a microtensile specimen of the same type as shown in the previous figure, that had been strained to failure. The dislocation density has increased by more than an order of magnitude.

Metal films below a minimum thickness in the range of tens to hundreds of nanometers tend to lack mobile dislocations. This conclusion has been reached both in analytical predictions and in experiments [53–55]. Figure 4.9 [16,52] shows a TEM micrograph of a tensile specimen in the thin region adjacent to the failure site. This specimen, again the same material as in the previous two figures, exhibited a chisel-point fracture. The material stretched by thinning, and then parted. Figure 4.9 shows that dislocations are absent from the region near the fracture, and reappear in the thicker region further away. Figure 4.9 also shows another feature, prismatic dislocation loops, which are immobile and therefore are retained in the failed specimen. These loops are the residue of clusters of vacancies; vacancies agglomerate as a disk, the flat surfaces bond together, and a dislocation is created as the boundary. The prismatic loops are the small, round structures that resemble coffee beans.

4.3.5. Electromigration and Voiding

Electromigration is the phenomenon of mass transport of metal atoms being driven out of a conductor by the flux of electrons impinging on each atom. Figure 4.10 [56] shows a void and a hillock created by electromigration in an aluminum line. Electromigration
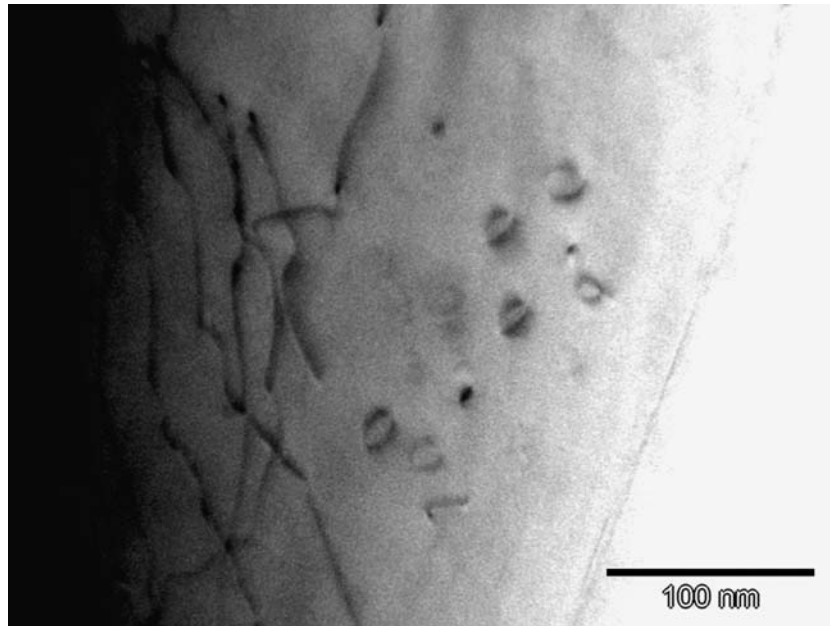
FIGURE 4.9. TEM micrograph of the failed edge of an aluminum thin-film microtensile specimen. The linear features on the left side of the image are dislocations; the thickness decreases from left to right in this image. The round features on the right are prismatic dislocation loops.
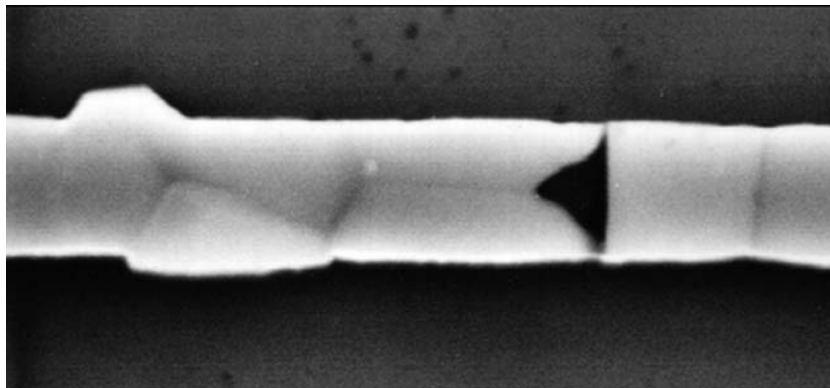

FIGURE 4.10. Hillock and void produced by electromigration in an aluminum line [56]. Reprinted by permission.

has been recognized as a reliability issue in integrated microelectronics devices for many years [57]. Tamura et al. [58] report on the stresses created by electromigration in copper. Stress and temperature affect electromigration. The stress effect operates to create a conductor length effect, as described by the Blech formula [5]. Conductive paths that are shorter than the "Blech length" do not fail by electromigration because the stresses created by electromigration itself, by moving atoms into a "crowded" region, are sufficient to halt the process. Standardized tests for electromigration have been developed; a thin-film con-
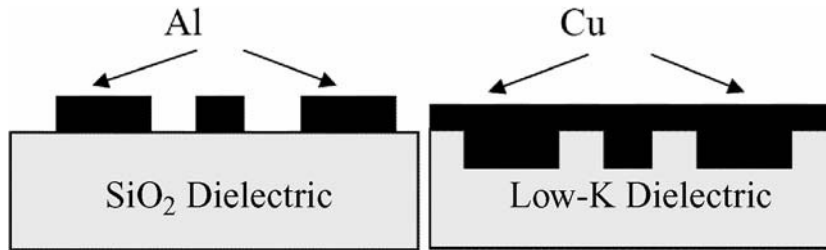
FIGURE 4.11. Schematics of Al/SiO$_2$ vs. Cu/low-k (damascene) interconnect structures.

ductor can withstand currents of 10 MA/cm^2 for short periods of time. Use of design rules that limit current densities to 0.1 MA/cm^2 controls electromigration in practical devices.

Thermal stress-induced voiding [59] is another diffusion-based reliability issue. It arises from high tensile hydrostatic stresses induced by encapsulation of metal lines in rigid dielectrics. Void growth is accelerated by increasing temperature and increasing stress.

4.3.6. Structural Considerations

The classic single-layer line-on-substrate design could not provide the interconnect density needed for large-scale integrated circuits, so multilevel interconnect structures became necessary decades ago. Interlayer dielectric films were applied over aluminum lines, via holes were patterned and tungsten vias placed, and the next layer of interconnect was deposited. However, for the new copper interconnect structures, a different design has been adopted, the damascene approach, Figure 4.11. The trenches are patterned first, and then Cu is electroplated on top of the sputter deposited barrier and Cu seed layers. Excessive Cu is removed by the chemical mechanical planarization (CMP) process. This is a combination of chemical and mechanical polishing that adds a new set of challenges to the mechanical integrity of the interconnect structure. Chemical mechanical planarization can also be used with Al technology; its widespread use with Cu layers allows for a larger number of interconnect layers, currently around 10, in the device, thus higher complexity and level of integration. Figure 4.12 shows perspective images of interconnect structures [60].

4.3.7. Need for Mechanical Characterization

Mechanical characterization is useful in design for reliability, material acceptance, and quality control. Challenges to the mechanical reliability of thin films in microelectronic devices can arise during manufacture and in service, from a variety of sources; the main source of the stress is usually differential thermal expansion. Additional factors such as diffusion (promoted by high temperature), high voltage, and electrochemical corrosion (promoted by humidity) can significantly accelerate the failure process. Microelectronic devices contain a variety of different materials, with different thermal expansion coefficients and different elastic properties. These materials are rigidly joined with each other, often as alternating layers atop a stiff silicon substrate. The chips are heated from ambient to operating temperature, e.g., around 90°C for a typical desktop computer, at least once for every on-off cycle. Changes in the mode of use, e.g., beginning and ending a numerically intensive calculation, can add more cycles. Each temperature change produces thermal stresses caused by differential thermal expansion among the materials of the chip. High stresses can occur in encapsulated lines and in the enclosing dielectric. Since the
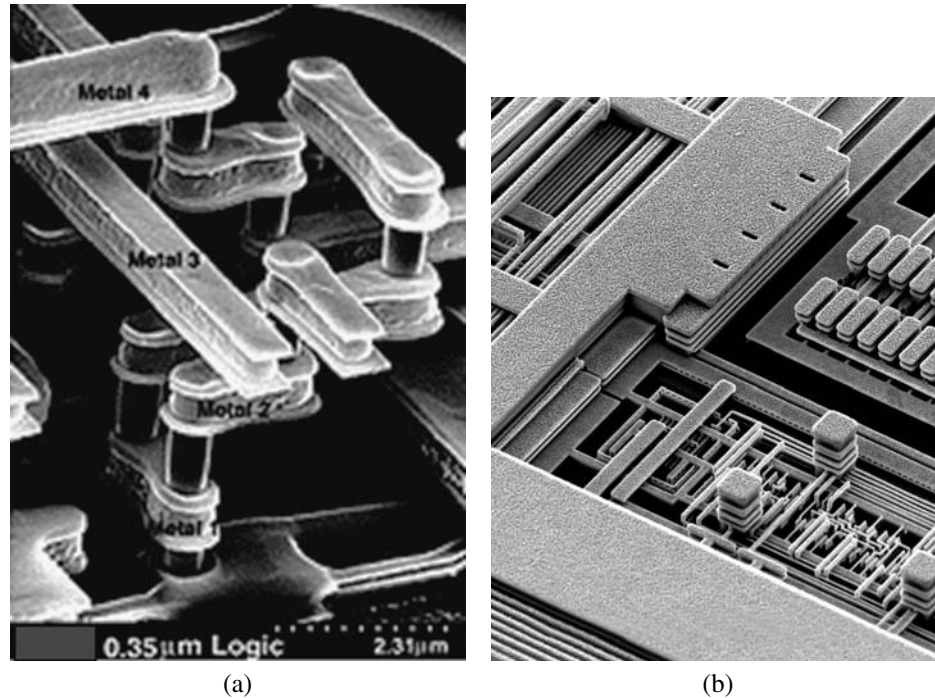
FIGURE 4.12. Aluminum (a) and copper (b) interconnect structures [60]. (b) Photo courtesy of International Business Machines Corporation. Unauthorized use not permitted.

processing speed increases with the current into and out of the transistors, high current levels are often favored. But, the higher the current, the higher the temperature, so commercial pressures favor devices capable of operation at high temperatures.

4.3.8. Properties of Interest

Here we focus on the set of properties needed in considerations of manufacturability and reliability of thin film structures, and specifically, on their measurement. Other properties, particularly electrical and optical properties related to the intended function of a film, are also of wide interest. Many of these can be measured on blanket films, or with straightforward test structures. Some properties of films, for example, the thermal expansion coefficient, are not measured; where data are needed, bulk properties are used. Mass density is becoming more important with the growing use of porous low-k (low dielectric constant) dielectric layers. However, the mass density of thin film layers is rarely measured directly, as discussed above.

Analytical or numerical simulation of the mechanical behavior of thin film layers relies on a handful of material properties, including Young's modulus or, in special cases, the anisotropic elastic constants, thermal expansion coefficient, yield strength, ultimate tensile strength, elongation to failure, residual stress, fatigue resistance in the form of stress-N or strain-N curves (where N is number of cycles), creep resistance, and adhesion. The differences from the design set for macroscopic structures are the importance of thermal expansion as a source of stress; the ubiquity of adhesion relative to joining; and the shift of fracture toughness issues from bulk materials such as welds to bimaterial interfaces. Thin

films in microelectronics devices have microstructures much different from those of traditional bulk materials. For metals, conventional wrought and annealed materials often have grain sizes in the tens of micrometers, while for films, sub-micrometer grain sizes are the rule. For polymers, the thin layers applied by spin- or dip-coating are likely to be different from extruded or cast bulk material. Polycrystalline silicon is not produced in bulk. Because material properties depend strongly on microstructure, characterization of thin films produced by the same deposition methods used in manufacturing of actual devices, and with specimens of the same general size scale as the films in actual devices, is necessary.

How can the values of these properties be obtained for a given material? Use of conventional mechanical testing instrumentation, such as the tensile test machine, for measurements on thin films is simply not appropriate. The films cannot be removed from their substrates for gripping, and the force sensitivity needed is orders of magnitude finer. The need for experimental techniques adapted specially for testing thin films has been recognized since at least the 1950's. The challenge of accurately measuring mechanical properties has stimulated the development of specimen designs and fabrication routes, and special test apparatus. The next section describes the most successful techniques for measuring mechanical properties of thin films.

4.4. METHODS FOR MECHANICAL CHARACTERIZATION OF THIN FILMS

The main methods in current use for mechanical characterization of thin films include microtensile testing (MT) and instrumented indentation, also referred to as nanoindentation (NI). Other methods in wide use include wafer curvature, the pressurized bulge test, and a variety of tests of the adhesion of a film to its substrate.

4.4.1. Microtensile Testing

Tensile testing is the standard means of obtaining mechanical properties of structural metals. Because the stress field is uniform throughout the gage section, the Young's modulus, yield strength, and ultimate tensile strength can be obtained from an accurate force-displacement record. So it was natural to apply this time-tested method to thin films. Early attempts to pull thin films in conventional testing machines used specimens lifted from the substrate; researchers encountered problems in placing the specimen on the grips without excessive wrinkling, and depended on special separation layers beneath the specimen film, such as water soluble sodium chloride. Early tests of metal films revealed the main phenomena still seen today: high strength, and low elongation to failure [61]. There is at present no standard test method for microtensile testing of thin films; individual investigators adapt the standard methods for bulk metal specimens to fit their specific specimen geometry. Standardization is hindered by the multitude of specimen sizes and designs that are in use, which has resulted from the difficulty of fabricating microtensile specimens.

The problems with the early methods led to improved procedures, and progress continues. It became evident that since films in actual devices are always produced on substrates, the use of the substrate to support the thin film specimen is appropriate. But the substrate is always much more massive than the film, so it must be removed at least from beneath the gage section of the specimen. Ding et al. [62] reported the use of a silicon frame design for testing doped silicon. The first realization of this scheme for metal films was the silicon frame tensile specimen [63]. Bulk micromachining of MEMS devices had
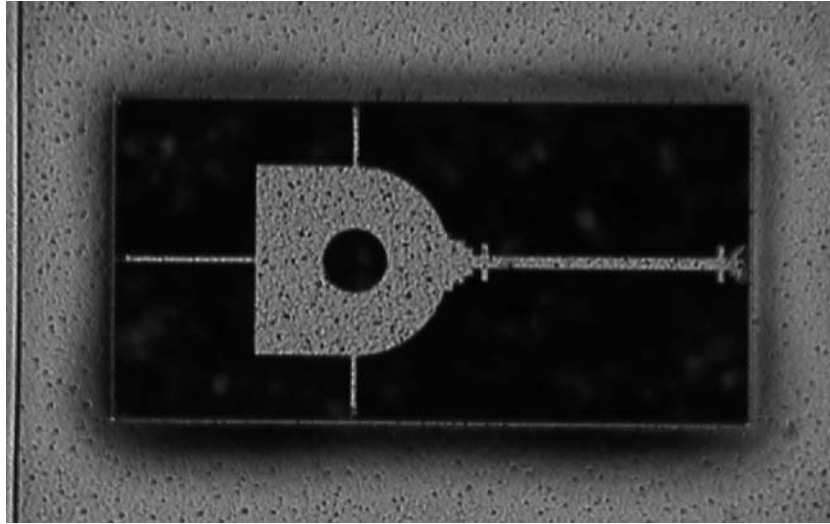
FIGURE 4.13. Microtensile specimen of aluminum, fabricated through the MOSIS process. The loading tab, with its 50 μm hole, is to the right. The gage section, with "ears" for use in digital image correlation for displacement measurement, is to the left. The silicon substrate has been etched away to a depth of 60 μm or more. The three slender aluminum lines connecting the field to the loading tab are tethers which are manually cut just before testing.

been developed by this time, demonstrating the concept of etching away a selected portion of the substrate to form a useful device. To produce the silicon frame tensile specimen, photolithographic patterning is used to form a straight and relatively narrow gage section with larger grip sections on a silicon frame. The substrate beneath the gage section is removed by a suitable etchant. The silicon frame, carrying its tensile specimen of a thin film, is mounted on a suitable test device capable of supplying force and displacement [64]. The silicon frame is cut, while leaving the specimen undamaged. This step has been accomplished manually with a dental drill, using a temporary clamp to hold the specimen in place, and by the use of a cutting wheel mounted on a movable stage [65].

All the MT techniques include measurements of force and displacement. The force is measured by a load cell, either commercial or custom-built. For the specimen introduced above, the force might amount to 0.1 N; commercial load cells with this range are available. Displacement has been measured by interferometric techniques such as electron speckle pattern interferometry (ESPI), for example as in [66], or by diffraction from markers placed on the specimen surface [67].

The specimen fabrication challenge with these techniques is the chemical selectivity required to etch through hundreds of micrometers of silicon without damaging the metal specimen. Aqueous hydrazine has been used, but this material is hazardous. Another disadvantage is the large width of the gage section, 100 μm or more, compared to the linewidths used in interconnect, and also compared to a typical film thicknesses of 1 μm.

A new generation of smaller-scale specimens and complementary test techniques has been developed. In this version, the specimen width is around 10 μm and the gage length is around 200 μm, while the thickness remains near 1 μm, Figure 4.13 [68]. The surface micromachining concept is used; the substrate is removed to a depth of around 100 μm beneath the specimen, using xenon difluoride. This etchant is less hazardous than hydrazine,
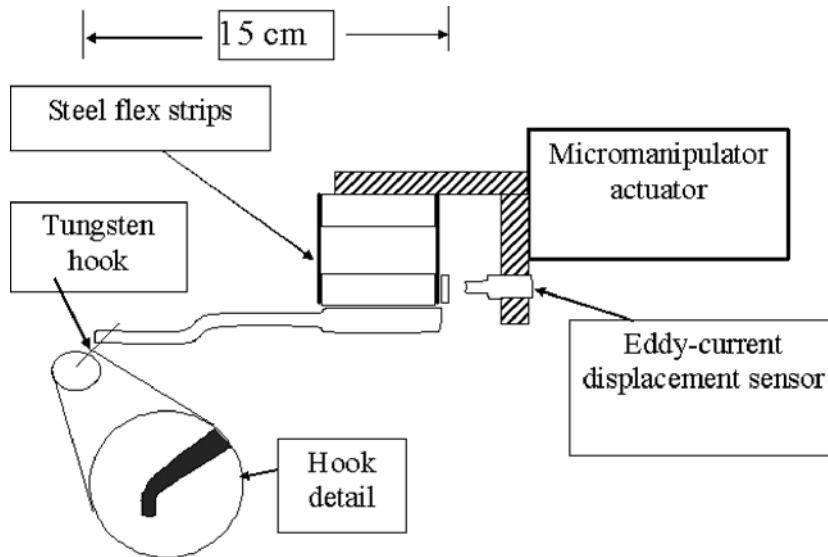
FIGURE 4.14. Tungsten "hook" carried by instrumented micromanipulator to load tensile specimen and measure the force.

and is very selective for silicon masked by SiO_2, aluminum, copper, etc. The control of edges; the elimination of the need to manually lift a film off a substrate, often with the aid of a water bath, and place it on tensile grips; and the use of specimens with aspect ratios (width to thickness) of 10 or less, have significantly mitigated the presence and effects of wrinkles and edge nonuniformity pointed out by Brotzen [69] in his review, discussed further below. Young's modulus can usually be measured in these specimens, but Poisson's ratio has been measured only by special techniques on relatively large specimens [70,71], because the transverse displacements are so small on a specimen only a few micrometers wide. In an early version of this test, the specimen was loaded by engaging a tungsten probe tip, 50 μm in diameter, to a hole in the loading tab, Figure 4.14. A recent variant of this technique is the membrane deflection tensile test, applied to a series of face-centered-cubic (FCC) metals by Espinosa et al. [72], Figure 4.15.

A new advance is the cofabrication of a specimen and a protective frame that includes a force sensor, Figure 4.16 [54]. This specimen is suitable for use inside a transmission electron microscope (TEM).

A recent round robin showed reasonable agreement among several laboratories in the strength of polySi, although most labs required their own unique specimen geometry. The different geometries were produced on the same MEMS chip [30]. The strength values obtained for polySi were impressively high, of the order of 1/30 of the polycrystalline Young's modulus, which is the usual estimate of the theoretical strength of a solid.

4.4.2. Instrumented Indentation

The nanoindentation test similar to the conventional hardness test, but is performed on a much smaller scale by use of specialized equipment—a nanoindenter [73]. The force, P, required to press a sharp diamond indenter into tested material is continuously recorded as a function of the indentation depth, h, as indicated schematically in Figure 4.17. The
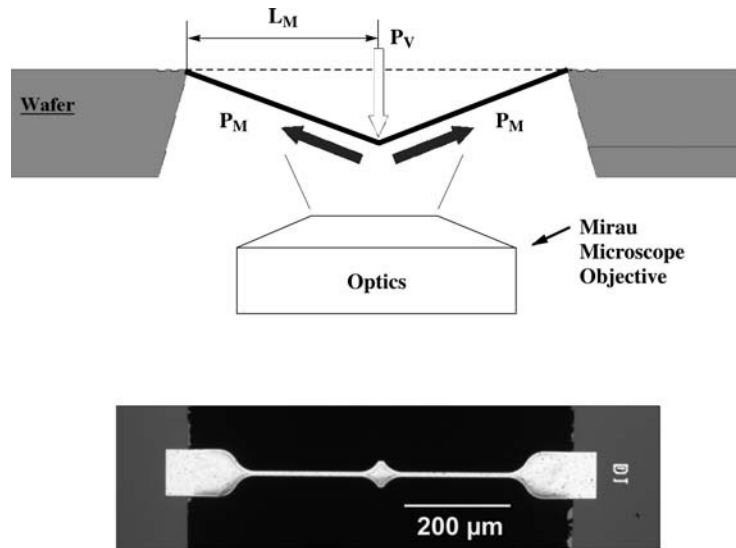
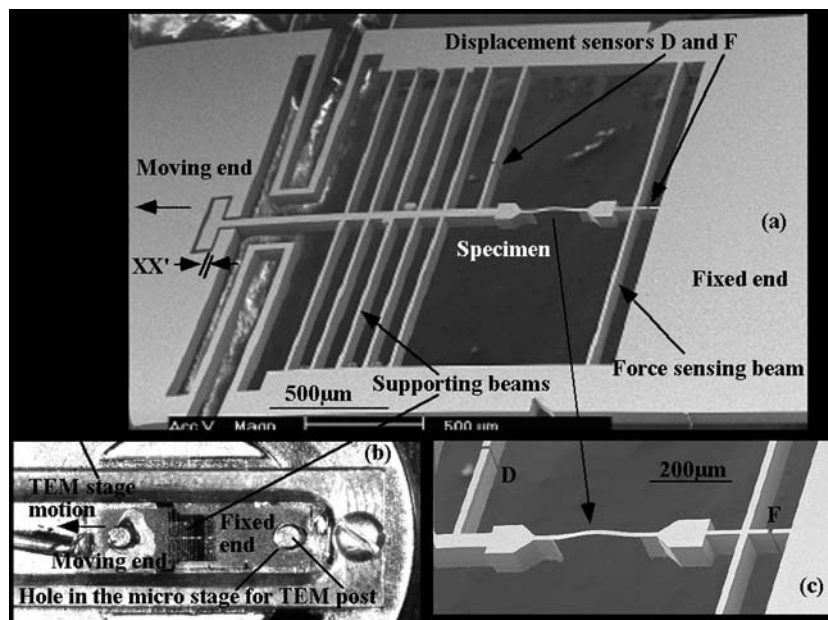FIGURE 4.15. Setup for the membrane deflection tensile test [72].

FIGURE 4.16. Tensile specimen assembly including aluminum tensile specimen and MEMS support assembly and force gage for use in the TEM [54].

actuation mechanism can be based either on electromagnetic or electrostatic application of force. Since the depth resolution is on the order of angstroms, it is possible to usefully indent even very thin ($\sim$100 nm) films. The nanoindentation load-displacement curve, similar to one shown in Figure 4.18, provides a "mechanical fingerprint" of the material's response to contact deformation. Elastic modulus and hardness are the two parameters that can be
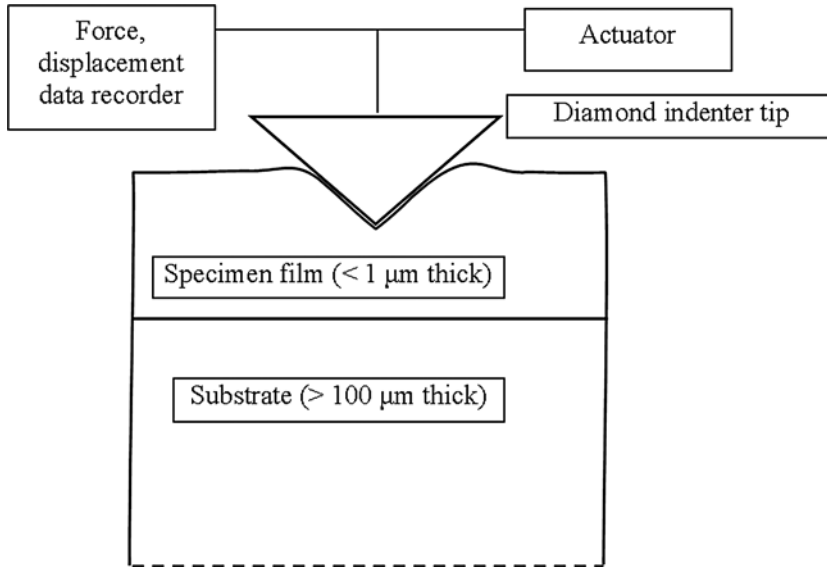
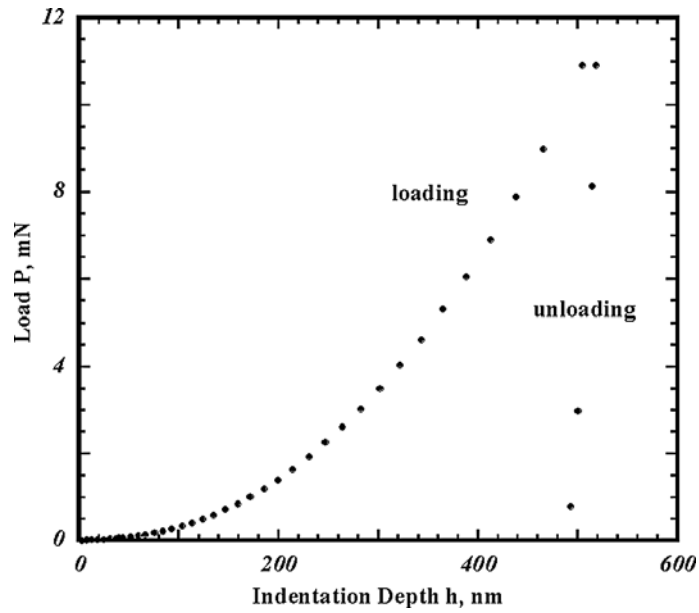FIGURE 4.17. Schematic of instrumented instrumentation apparatus.

FIGURE 4.18. Load-displacement record from an instrumented indentation test of an electrodeposited Cu film 1 μm thick.

readily extracted from the nanoindentation load-displacement curve. Elastic property measurements by nanoindentation were originally proposed by Loubet et al. [74]. Later, Doerner and Nix [75] suggested that a linear fit to the upper 1/3 of the unloading portion of

the indentation curve could be used to determine film stiffness, $S = dP/dh$, from which the reduced elastic modulus, E_r, could be found as

$$E_r = S \frac{\sqrt{\pi}}{2\sqrt{A}}, \tag{4.3}$$

where A is the contact area and E_r is a combined elastic property of the film and indenter materials. Since the indenter material itself has finite elastic constants, its deformation contributes to the measured displacement. The reduced modulus E_r, is given by:

$$\frac{1}{E_r} = \frac{1 - v_i^2}{E_i} + \frac{1 - v_f^2}{E_f}. \tag{4.4}$$

In this equation E is the elastic modulus, v is the Poisson's ratio, and the subscripts f and i refer to the film and the indenter materials respectively. A more elaborate power law fit to the unloading portion of the load–displacement curve was suggested by Oliver and Pharr [76], and is widely known as the Oliver and Pharr method.

Hardness H, a material's resistance to plastic deformation, is defined as

$$H = \frac{P_{\max}}{A}, \tag{4.5}$$

where A is the projected area of contact (a function of the indentation depth) at the maximum load $P_{\max}$.

The expressions for both elastic modulus and hardness contain the contact area, which is correlated to the indentation depth both theoretically, through the known geometry of the indenter, and experimentally, by indenting a material with known elastic modulus. This tip calibration procedure consists of indenting a standard material (often fused quartz or single crystal Al) to various maximum indentation depths. Since the contact area is determined from tip calibration, various tip geometries can be used, with the most common being the Berkovich three-sided pyramid geometry. From the manufacturing standpoint, a three-sided pyramid always ends as a point, and the tip radius can be as sharp as 10–50 nm. Other geometries are also used, and include Vickers (a standardized square pyramid), cube corner, conical and wedge indenters. The unloading slope, dP/dh, is related to the tip geometry as

$$\frac{dP}{dh} = 2\beta \sqrt{\frac{A}{\pi}} E_r, \tag{4.6}$$

where h is the indentation depth, and β is a constant, near unity for a given tip geometry. King et al. calculated β values for different tip geometries using finite element analysis [77].

One should note that the tip calibration does not account for either plastic pile-up or sink-in of both the standard and the specimen materials, which causes inaccuracies in indentation depth and contact area determination. In addition, the total test compliance, i.e., the inverse of stiffness, is affected by the indentation contact. One should also account for the test frame compliance, C_f, as it offsets the total test compliance:

$$C_{total} = C_f + \frac{\sqrt{\pi}}{2\sqrt{A} E_r}. \tag{4.7}$$

In order to avoid substrate effects on the measured mechanical properties, a film should be indented only up to a certain percentage of its thickness (up to 10–20%). There is also an influence of the residual stress and substrate effects that are hard to account for in the analysis [78,79]. Indentation curve analysis has been extended in the past few years with new FEM-based models being developed [80,81].

A more powerful variant of the indentation technique uses a "continuous stiffness" approach (continuous stiffness method, CSM, in which the contact stiffness is measured by multiple small (2 nm) loading and unloading cycles (0.5 to 300 Hz) superimposed on the load-displacement curve. The original idea was proposed by Pethica and Oliver [82], where they used a force controlled indenter, superimposing a small sinusoidal component on the quasistatic indentation load. This resulted in the indenter displacement phase shift with respect to the excitation force:

$$\tan(\phi) = \frac{\omega D}{\dfrac{SK_f}{S + K_f} + K_s - m\omega^2},$$ (4.8)

where ϕ is the phase angle, ω is the frequency of oscillation, m is the mass of the indenter tip, Figure 4.19, $K_f = 1/C_f$ is the stiffness of the load frame, K_s is the spring constant of the indenter support springs, and D is the damping coefficient. The contact stiffness can be calculated from [76]

$$\frac{\Delta P}{h(\omega)} = \sqrt{\left(\frac{SK_f}{S + K_f} + K_s - m\omega^2\right)^2 + \omega^2 D^2},$$ (4.9)

where ΔP is the magnitude of the force oscillation, and $h(\omega)$ is the magnitude of the displacement oscillation.

Both elastic modulus and hardness can be calculated for the unloading portion of each tip oscillation during indentation. Figure 4.20 shows elastic modulus and hardness obtained with the CSM method for a 1 μm thick electroplated Cu film on a Si substrate.
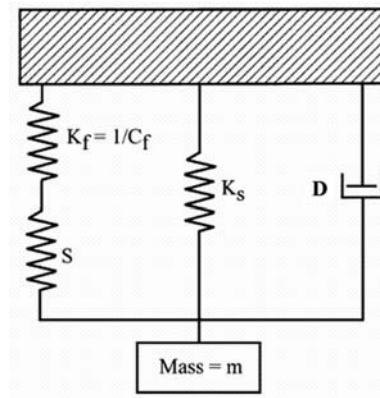

FIGURE 4.19. Schematic of the indentation dynamic model (adapted from [23]). K_f is the stiffness of the instrument frame, S is the stiffness of the tip-specimen contact, K_s is the stiffness of the springs that support the tip, D is the damping coefficient, and m is the mass of the tip assembly.
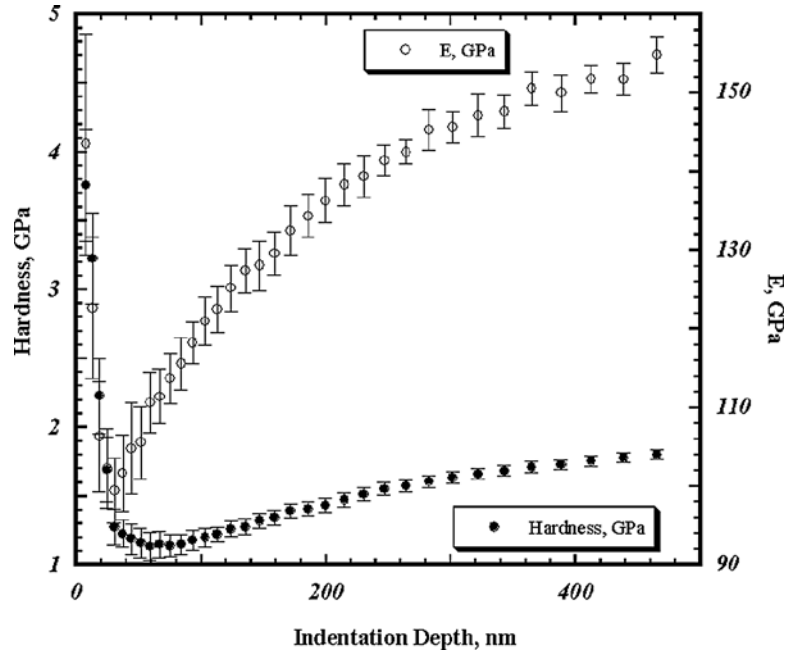
FIGURE 4.20. Elastic modulus and hardness for a 1 μm thick electroplated Cu film on Si substrate measured using continuous stiffness method.

Here, the substrate effects can be seen at a depth of 50 nm for the modulus, and 100 nm for the hardness. On the one hand, this is an advantage, as composite properties of the film and the substrate are measured. On the other hand, extrapolating "true" film mechanical properties from such data can be challenging. Here, the free-standing film tensile techniques are advantageous. A comprehensive review of the method applied for magnetic storage and MEMS was reported by Li and Bhushan [83].

4.4.3. Other Techniques

4.4.3.1. Wafer Curvature   The basic principle of the wafer curvature technique is that differential thermal expansion between a specimen film and a silicon substrate produce measurable curvature of the substrate (the wafer); the curvature is related directly to the product of stress and thickness in the film, through the Stoney equation, discussed above. This phenomenon is used in evaluating and adjusting film deposition procedures, to measure residual stress in the deposited films. High values of residual stress, especially tension, may make a film less resistant to delamination from the substrate.

Wafer curvature measurement was adapted for characterization of mechanical behavior by Nix [84]. The substrate with its film is placed in a furnace equipped for measurement of the substrate curvature. The temperature is cycled, while the curvature is recorded. Given the film thickness, the film stress can be plotted against temperature. The accessible range of temperature is limited only by the eventual breakdown of the specimen film by melting or chemical reaction. The stress depends in turn on the difference in thermal expansion between the specimen film and the substrate, and the elastic constants of the specimen film. Deviations from linear behavior with temperature imply plastic deformation of the specimen film; the nature of this deformation is confirmed by the hysteresis loop observed at
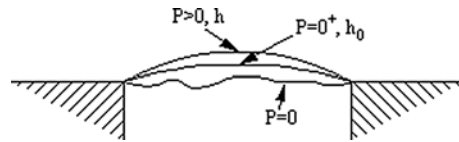
FIGURE 4.21. Schematic diagram of the bulge test specimen, showing a slack film loaded with zero, infinitesimal, and finite pressure.

least on the first temperature cycle. The advantages of the wafer curvature technique include the simplicity (in principle) of both the experimental technique and the specimen, which is a film on the same substrate used in actual manufactured products, without the necessity of selectively removing the substrate beneath the film. Analysis of the results does not require knowledge of the elastic properties of the deposited film, only those of the substrate. The disadvantages are that (1) the ultimate tensile strength and elongation to failure cannot be measured, and that (2) only certain combinations of Young's modulus, flow stress, and temperature are accessible. This technique has been very successful in providing insight and data on deformation mechanisms particularly in aluminum films [84].

4.4.3.2. Pressurized Bulge Testing   The name of the pressurized bulge test is descriptive: by etching away the substrate beneath a region of the specimen film, the film can be exposed to stress by a pressurized fluid introduced beneath the substrate. The mechanics of a pressurized membrane can be used to analyze the observed behavior. The shape of the pressurized region is chosen intentionally; circular, square, and rectangular shapes have been explored. The out-of-plane deformation of the membrane can be measured by interferometry or related optical techniques. This technique has been used to explore the elasticity of thin films; care must be taken to properly characterize the initial state of the film, including the possibility of residual stress, Figure 4.21 [85,86]. It has also been used to measure the adhesion between the film and the substrate [87].

4.4.3.3. Deformed and Resonant Cantilever   Micromachined cantilevers have been used as specimens in thin film properties measurements [29,88]. Photolithography can be used to define the cantilever geometry. Cantilevers can be deformed by loading with, for example, an instrumented indenter, or can be excited to resonance, to measure film elastic properties. The relationship between the mechanical stiffness or the resonant frequency and the elastic constant of the film depends sensitively on the dimensions of the cantilever [89]. The ideas of the bulge test and resonance can be combined in the resonant membrane test, which can be used to determine the product of film elastic modulus and mass per unit area. If the thickness and mass density of the film are known, the elastic modulus can be extracted.

4.4.4. Adhesion Tests

Adhesion between layers of different materials is a critical issue in microelectronic packages, and also within the chips. While the time-honored "scotch tape" adhesion test is still in use, quantitative tests, developed in recent years based on the concepts of fracture mechanics, provide material characteristics that can be compared to calculable stress- and strain-based driving forces, and are therefore suitable for use in lifetime predictions [90]. Reviews by Volinsky et al. [91] and by Lane [92] provide useful summaries. The basic idea, as in macroscale fracture mechanics, is that it is useful to quantify the conditions under which an existing crack may advance. The crack, in this case, is assumed to be a small delamination of the film from the substrate. The driving force for crack propagation
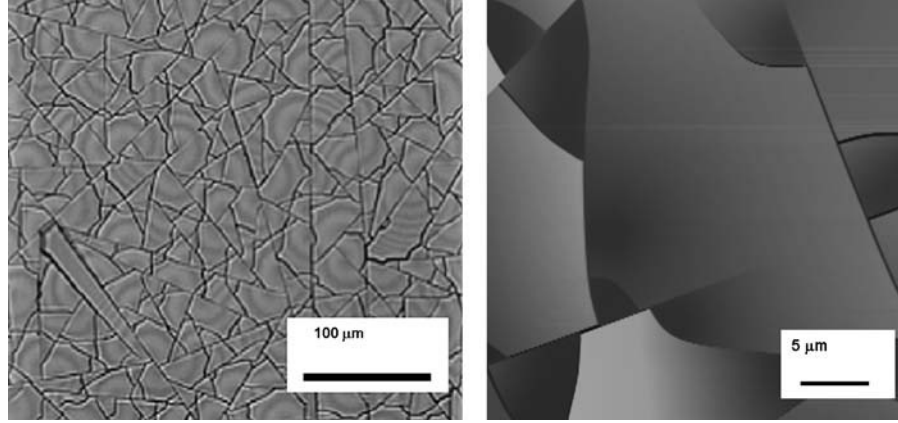
FIGURE 4.22. Optical and AFM images of cracks in low-k dielectric thin film.

is taken as the strain energy release rate, which depends on the geometry and the stress state. Both tensile and compressive stresses in thin films promote adhesion failures; a thin film in compression buckles, delaminates and spalls from the substrate when its strain energy release rate exceeds a critical value that is characteristic of the adhesion between film and substrate [93]. A general, simplified form of the strain energy release rate, G, in a stressed film, regardless of the algebraic sign of the stress, is:

$$G = Z \frac{\sigma_f^2 h}{E_f},$$
(4.10)

where σ_f is the stress in the film, h is the film thickness, E_f is the modulus of elasticity, and Z is a dimensionless cracking parameter. More accurately, the energy release rate averaged over the front of advancing isolated crack is

$$G = g(\alpha, \beta) \frac{\pi(1 - \nu^2)\sigma_f^2 h}{2E_f},$$
(4.11)

where $g(\alpha, \beta)$ is a function of the Dundurs parameters α and β, and can be found in [94,95]. This strain energy release rate is the driving force for fracture. Film fracture or delamination is observed when the strain energy release rate exceeds the toughness of the film, G_f, or the interfacial toughness, Γ_I respectively ($G > G_f$, or $G > \Gamma_I$). One can avoid these types of failures by either reducing the film thickness, or the stress, or by increasing adhesion. Practically, the film thickness is easier to control. For a given stress level, there is a certain critical film thickness, at which failures are observed. As an example, Figure 4.22 shows through-thickness cracks in a low-k dielectric film 2 μm thick. Thinner films showed no signs of failure.

In case a film has fractured, and its residual stress and thickness are known, Equations (4.10) and (4.11) can be used as upper bound estimates for adhesion. For example, the 1 μm TiWN film on a GaAs wafer had adhesion of at least 5 J/m^2, having the maximum residual stress of 1 GPa, as seen in the stress map in Figure 4.3.

In the case of a compressed films, telephone cord delamination is commonly observed (Figure 4.23). The geometry of the buckles can be used to asses thin film adhesion.
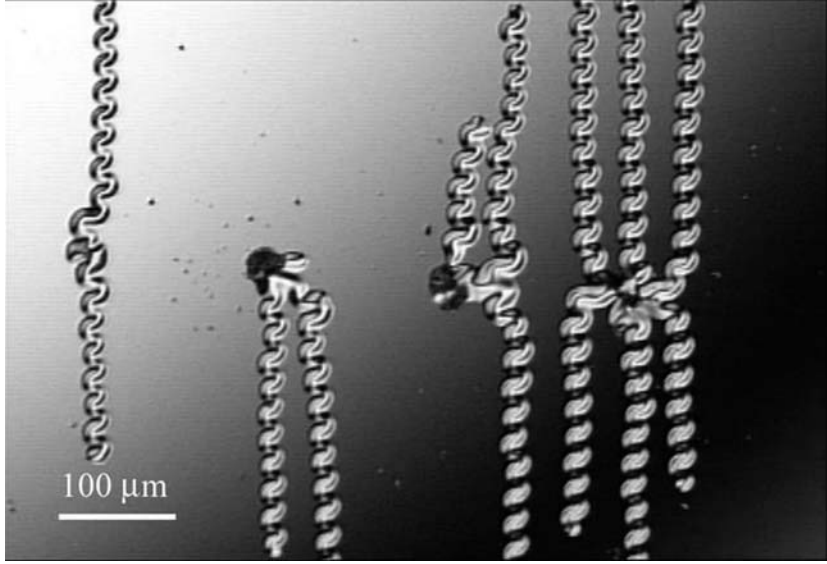
FIGURE 4.23. Telephone cord delamination in a 1 μm tungsten film.

The following analysis is based on Hutchinson's and Suo's developments for buckling-driven delamination of thin films [96]. Upon buckling, the stress in the film, σ_B, is estimated as

$$\sigma_B = \frac{\pi^2}{12} \frac{E}{(1 - \nu^2)} \left(\frac{h}{b}\right)^2, \tag{4.12}$$

where h is the film thickness, b is the blister half-width, and E and ν are Young's modulus and Poisson's ratio, respectively. The buckling stress is acting in the vertical direction, perpendicular to the straight blisters shown in Figure 4.24(a). Here, the buckling stress of the W film is estimated to be 275 MPa.

The compressive residual stress, σ_r, responsible for producing buckling delamination is

$$\sigma_r = \frac{3}{4} \sigma_B \left(\frac{\delta^2}{h^2} + 1\right), \tag{4.13}$$

where δ is the blister height [Figure 4.24(b)]. For the example presented in Figures 4.23–4.24, a 1.9 GPa residual compressive stress is estimated, in good agreement with the measurements of wafer curvature and X-ray diffraction stress performed on the non-delaminated samples.

The film steady state interfacial toughness in the direction of blister propagation [Figure 4.24(a)] was estimated as

$$\Gamma_{SS} = \frac{(1 - \nu^2) h \sigma_r^2}{2E} \left(1 - \frac{\sigma_B}{\sigma_r}\right)^2, \tag{4.14}$$
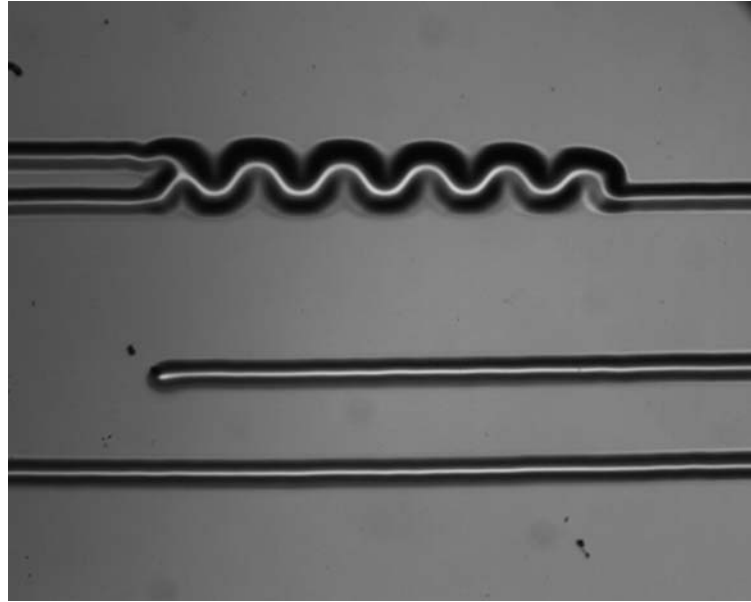
(a)
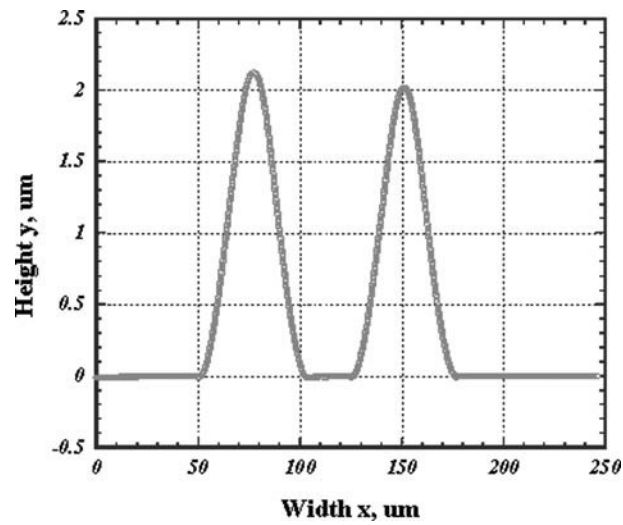
(b)

FIGURE 4.24. Analysis of the telephone-cord delamination of a tungsten film shown in the previous figure. (a) Telephone cord delamination in a 1 μm tungsten film on top of a 2 nm diamond-like carbon (DLC) film on Si. (b) Corresponding blister heights profile.

which gave 3.6 J/m^2 in this case. Mode-dependent interfacial toughness in the buckling direction, perpendicular to blister propagation is

$$\Gamma(\Psi) = \frac{(1 - \nu^2)h}{2E}(\sigma_r - \sigma_B)(\sigma_r + 3\sigma_B), \tag{4.15}$$

giving 6 J/m^2. This is in agreement with the superlayer indentation adhesion test result of 6.4 ± 0.4 J/m^2 [97].

The superlayer indentation test provides information on local film adhesion at the microscale. A superlayer film, selected for high stress, high strength, and high adhesion, is deposited on top of the film to be tested. Indentation is used to initiate delamination. The highly stressed hard superlayer provides additional driving force for interfacial crack propagation, and prevents plastic deformation of the tested film around the indenter. As the indenter tip is pressed against the superlayer film stack, it supplies additional energy necessary for crack initiation and propagation. The blister radius is measured optically, Figure 4.25(a). The indentation volume is obtained from the plastic depth of the load-displacement curve [Figure 4.25(b)] and the tip geometry. Both the blister radius and the indentation volume are then used to calculate the strain energy release rate (measure of the practical work of adhesion). Calculations for adhesion measurements were made by following the solution developed by Marshall and Evans [98] that was further expanded by Kriese and Gerberich et al. for multilayer films [99,100]. Figure 4.25(a) shows a typical delamination blister seen from making indents with a conical tip at 300 mN maximum load and a corresponding load-displacement curve. From Figure 4.25(b), the plastic indentation depth is obtained by using the power law fit of the top 65% of the unloading curve [76], and used to calculate the indentation volume, based on the tip geometry. It is assumed that the volume is conserved, and plastic deformation around the indenter results in the elastic displacement at the crack tip, allowing calculation of the indentation stress, and ultimately the strain energy release rate, a measure of the practical work of adhesion. Adhesion results for several film materials relevant to microelectronics are summarized in [101].

Moisture has been known to reduce the fracture toughness in bulk glasses [102], as well as causing failures in mirrors [103]. Figure 4.26 shows buckling delamination in a mirror backing layer that is over 200 years old. Similar effects are observed in thin films [97]. This becomes extremely important, as the films are exposed to moist and corrosive environments during processing (e.g., CMP). Figure 4.27 shows water-induced delamination of a tungsten film; telephone cord propagation of the delamination is seen in the upper portion *vs* no cracking on the dry lower portion. The modified superlayer indentation test conducted in moist environment showed an adhesion decrease up to 60 times compared to the tests in dry lab environment. In this case environmentally assisted fracture is observed; the Γ_I interfacial toughness term is decreased by the presence of water, so that the failure condition $G > \Gamma_I$ is met.

Because the interfacial energies found in films are numerically much lower than those in bulk metals, for which fracture toughness testing was developed, the four-point-bend bar with a cracks propagating along its length from a central notch has been found useful [90,104–106]. Below we briefly describe this technique, to show a specific application of fracture mechanics in thin film adhesion. The many reports of adhesion measurement methods in the literature are a testament to the importance of the problem, the difficulty of the measurement, and the ingenuity of the researchers. However, a detailed review is beyond the scope of this article.

The delaminating beam test specimen, Figure 4.28, is a four-point-bend bar with an interface of interest built into the interior of the beam along the whole length. A "sandwich" beam made with the substrate on the top and bottom, and the surface layers bonded together in the center, is a typical geometry. The substrate layers are much thicker than the interface layer, and give the assembly sufficient stiffness to handle. In the bending beam, the outer fiber in tension is often located on the upper side, and is conventionally referred
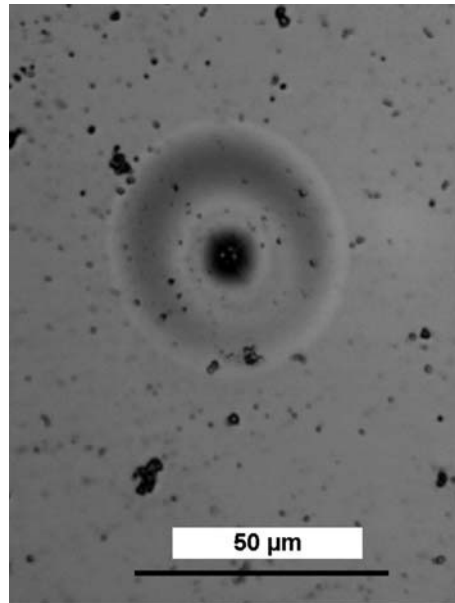
(a)
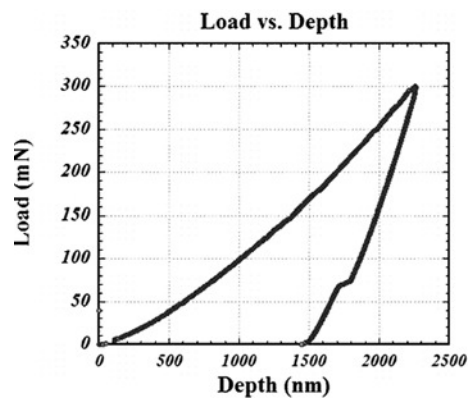
(b)

FIGURE 4.25. (a) Indentation-induced delamination blister in tungsten film; and (b) corresponding load-displacement curve.

to as the top of the specimen. The bottom fiber is in compression. The top section is carefully cut, without notching the bottom section. Cracks are intentionally nucleated to grow away from the notch along the interface layer being tested. While the crack length significantly exceeds the thickness of the cut layer, steady state energy release rate obtains, until the cracks reach the inner loading points of the four-point-bend specimen. The energy release rate is evaluated from the load and displacement, specimen geometry, and elastic properties of the support layers of the specimen. An advantage of this test is that the parameters needed to evaluate the adhesion do not include the residual stress on the film, which may be difficult to measure. Becker et al. [106] point out that properties measured with this specimen may depend on the specific geometry, contrary to the case for standard-
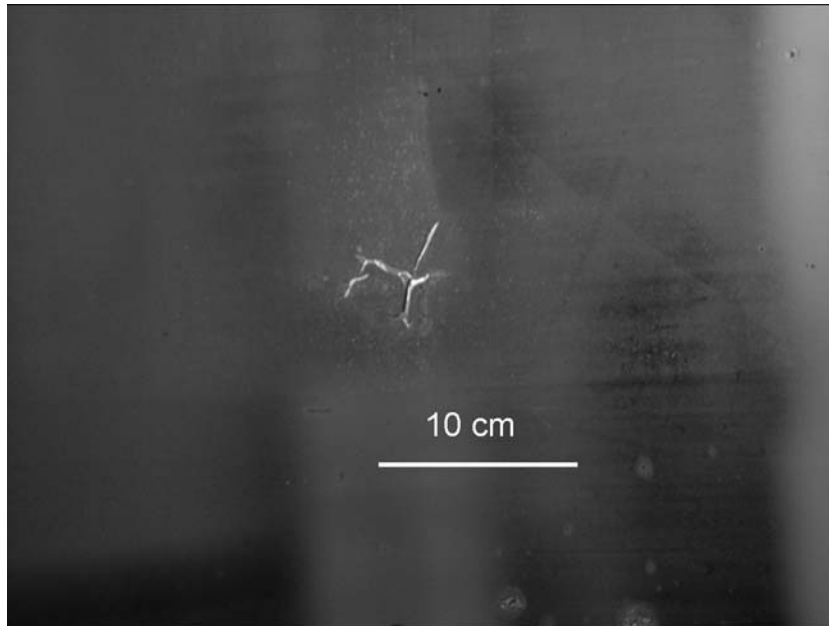
FIGURE 4.26. Environmentally assisted fracture in an antique mirror 200 years old.
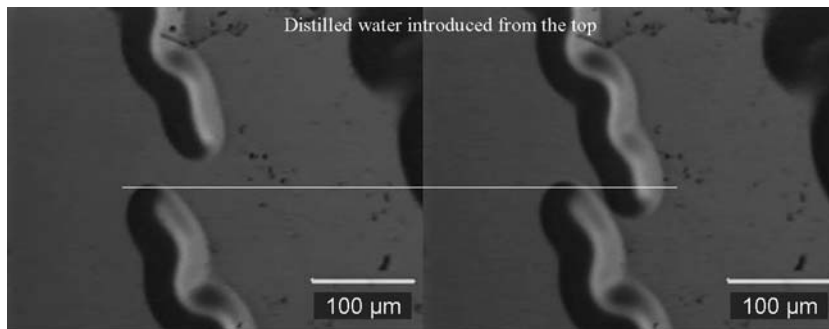
FIGURE 4.27. Water-induced blister growth. The image on the left shows blisters before water was introduced; the image on the right, after. The water was introduced from the direction of the top of the figure. The blister at the top (wet side) grew noticeably toward the lower side of the figure, while the blister at the bottom (dry side) did not grow.

ized fracture toughness specimens. This is not considered to be a serious disadvantage for testing materials for chips and electronic packages, because actual-size specimens can be tested.

All the fracture toughness techniques highlight a critical problem in the design of electronic packages and chips: some commonly used interfaces, such as polymer–metal interfaces, have very low fracture toughness, around 10 J/m^2 [90].

FIGURE 4.28. Delaminating beam specimen for measuring the energy required to separate an adhesive interface.

4.5. MATERIALS AND PROPERTIES

Reviews of the mechanical properties of thin films have appeared over the years [61,69]. The general conclusions formulated by Brotzen [69] are still relevant:

1. The elastic properties of thin films ordinarily do not differ greatly from bulk properties, and Young's moduli measured by various techniques do not differ greatly.
2. The thinner the films, the greater are the hardness and strength.
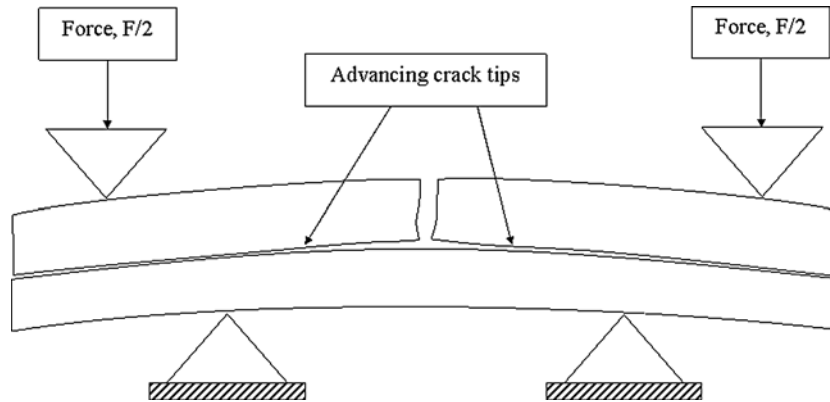3. Specimen preparation methods and the structure of the films have a significant effect on the mechanical properties of the films.

Item 3 above should be applied as a cautionary remark to both previous items. Brotzen's conclusions will be adopted as "rules of thumb" for discussing and interpreting the measured properties of thin films. Application of these rules to some example cases will be discussed below.

4.5.1. Grain Size and Structure Size Effects

4.5.1.1. Hall-Petch Rule   A useful general rule for strength properties of ductile metals is the Hall-Petch rule [107], which states that strength increases with the inverse square root of the grain size. In thin films the grain size often varies in the same direction as the film thickness, so rule 2 above can be seen as a special case of Hall-Petch behavior. Additional effects produced by the film-substrate interaction have been described, which tend in the same direction, that is, strength increases as the controlling size scale decreases. The small grain size usually present in thin films explains the common observation that thin films have higher strengths than bulk materials of the same chemical composition. Film strengths are usually portrayed as consistent with those of bulk materials when the grain sizes are considered.

Clearly the Hall-Petch rule must break down at some small grain size, because the size cannot be smaller than a single atom. Such a change in behavior has been detected recently at grain sizes of a few nanometers, although it is not yet clear whether the strength peaks or reaches a plateau. A set of data showing a clear peak in hardness at 11 nm was reported by Conrad and Narayan [108]. A molecular dynamics study by Schiotz and Jacobsen [55] provides some insight into the mechanism.

4.5.1.2. Low Elongation to Failure   The effect of film thickness on elongation to failure in microtensile tests has not been explained in detail. Elongation is one of the measurements recorded in tensile tests of bulk materials; it is an indicator of a material's ductility and capacity for absorbing energy before fracture, and hence its fracture toughness. In bulk materials, values of 10% or more are common, and values exceeding 100% are possible. Metal thin films, often made using very pure starting materials, commonly exhibit very low elongation to failure in tensile tests. An elongation to failure of 1% for a specimen of copper or aluminum 1 μm thick is typical. This result is not commonly interpreted to mean that the film lacks the capacity for plastic deformation, but rather is considered to be a geometric effect. Deformed regions, once formed, reduce the area of the film locally, and do not work-harden enough to prevent additional deformation from accumulating. Specimens of polyimide [109], and of aluminum deposited under unusual conditions [68], have shown substantial elongation. Microscopic examination of the failed region in metal films, for example, by scanning electron microscopy (SEM), often shows fine-scale features characteristic of high local ductility, such as ligaments [110].

4.5.1.3. Young's Modulus   Brotzen [69] comments at length on modulus values reported for bimaterial multilayer films with layer thicknesses of the order of nanometers. The situation appears to be that these bilayer films exhibit variable elastic properties as a function of layer thickness, but the variations are more modest than spectacular. A different type of modulus variation, the modulus deficit, was reported by Huang and Spaepen [111]. Here the relevant rule is number 3; film microstructure and morphology are the controlling features. Measurements of the density of thin films are difficult and are not commonly made. Porosity or voiding between grains is possible for some film deposition methods. Clearly a porous film may have an elastic modulus lower than a fully dense film of the same thickness. However, there are recent indications [112] that the typical expectation that the modulus deficit should be related to the porosity by a numerical factor near unity, as given by the results of Kachanov et al. [113], may underestimate the effect.

4.6. PROPERTIES OF SPECIFIC MATERIALS

Fabrication methods and test techniques for some widely used thin film materials have become sufficiently widespread that specific values of the properties can be usefully given. Of course, Brotzen's rule 3 still holds: the microstructure and chemical composition of the specific material at hand determine its properties.

Mechanical properties of selected thin materials as measured by microtensile testing or nanoindentation are listed in Table 4.2.

The practicality of the instrumented indentation test is a main reason for its widespread implementation. Of the two mechanical property values produced by the NI test, Young's modulus and hardness, only the Young's modulus is comparable to values produced by microtensile testing; even for the Young's modulus, conversion from the measured biaxial modulus is needed for comparison to handbook values. Limitations of applicability of the NI test, related to the film thickness and the relative stiffness of the film and the substrate, are being studied in current research. The high values of hardness produced in the NI tests, commonly reaching over 1 GPa, and occasionally over 10 GPa, are strikingly different from the strength values obtained by microtensile testing, Table 4.2. A basic rule of thumb is that the hardness value produced by indentation should be three times the stress value at some selected value of strain in the tensile test. The relevant strain value is sometimes given as 8%, but, as shown in Table 4.2 above, thin films rarely reach 8% strain in

TABLE 4.2.

Mechanical properties of selected thin films as measured by microtensile testing or nanoindentation.
See notes below.

Material	Fabrication method	Thickness, μm	Yield strength, MPa	Ultimate tensile strength, MPa	Young's modulus, GPa	Elongation to failure, %	References
Microtensile results							
Al	sputtered	0.05	327		62[a]		[114]
Al	sputtered	0.1	700				[114]
Al	sputtered	0.2	330		70		[114]
Al	e-beam evaporated	0.2	205	375[b]	65–70		[72]
Al	e-beam evaporated	1	150		65–70		[72]
Al	e-beam evaporated	1	94	151	24–30	22.5	[68]
Al-0.5%Cu	MOSIS[d]	1.5 and 2.4	65	74	40	1.4	[115]
Cu	e-beam evaporated	0.2	345		125–129		[72]
Cu	e-beam evaporated	1	160[c]		125–129		[72]
Cu	electrodeposited	9.7	253	311	67		[116]
Au	e-beam evaporated	0.3, 0.5	220		53–55		[72]
Au	e-beam evaporated	1	90		53–55		[72]
Ni	electrodeposited	4.7		1516	102–114		[117]
Polyimide	Spun on, baked	0.6	103	181	5.5	24	[109]
PolySi	MUMPS 25, 30[d]	3.5	NA	0.95 GPa	157		[71]
PolySi	SUMMiT[d]	2.5	NA	3 GPa			[30]

Nanoindentation results						
Material	Fabrication method	Thickness, μm	Yield strength, MPa	Hardness, GPa	Young's modulus, GPa	References
Cu	electrodeposited, annealed	0.5		1.04–1.27	121–132	[118]
Cu	electrodeposited, annealed, polished	0.5		1.21–1.29	131–138	[118]
Cu	electrodeposited	0.2 to 2	530 to 330			[23]

The study by Espinosa et al. [72] is quoted extensively here because it is recent, uses consistent methods on gold, aluminum, and copper films, includes specimen thickness and width effects, and includes considerable microstructural characterization and post-test observations of the specimens.

[a] The authors remark that this value shows the effect of film thickness on Young's modulus. If correct, this would be one of the first experimental demonstrations of this theoretically predicted effect.

[b] Unusually high value for this material and thickness.

[c] Unusually low value for this material and thickness.

[d] Special proprietary deposition process; sources identified in the references.

microtensile tests. A more detailed study of the extraction of yield strength values from nanoindentation tests was reported by Kramer et al. [119].

4.7. FUTURE RESEARCH

4.7.1. Techniques

The experimental convenience of the nanoindentation test, combined with its focus on key properties, modulus and hardness, and its ability to produce a quantitative and reproducible force-displacement record, has made it widely popular. Outstanding problems include the derivation of design properties, such as yield strength, from nanoindentation data. Detailed data on typical features of the nanoindentation test, such as sink-in and pile-up, are being sought to help clarify the interpretation of the results. The microtensile test requires patterning of a test structure, but offers less ambiguous measurements of the yield and ultimate tensile strengths, along with an indication of elongation to failure and a fracture surface which can be examined by TEM. More generally, the perennial problem of the expense of fabrication of test structures seems to weigh heavily against the routine measurement of mechanical property values of thin films.

4.7.2. Properties

The difficulty of measuring adhesion in multilayer thin film structures, and criticality of this property for reliability, seem to offer an opportunity for improved measurement techniques. Nanoindentation has been applied to the measurement of adhesion [91], but more extensive data are needed to demonstrate the generality and usefulness of this approach to adhesion. The fracture mechanics based tests appear to be easier to analyze, at the cost of preparation of the bend bar specimens.

Some test techniques have found Young's modulus values that differ from bulk values in some cases. The scientific issue of whether or not thin films have Young's modulus values different from bulk materials has been settled; any film with a substantial number of atomic layers, meaning, 20 or more, should have elastic properties indistinguishable from those of a bulk specimen of the same microstructure. This implies that the elastic properties of thin films can now be regarded as probes of the microstructure. Microstructural features that may affect elastic behavior include mass density and, for metals, the volume and behavior of material effectively in grain boundaries.

4.7.3. Length Scale

The effects of "length scale" on mechanical behavior have received intense study recently, e.g., [120]. A complementary view is that fine-scale microstructural variation may become significant when an experiment samples the behavior of very small volumes of material, for example, the material under the sharp tip of a nanoindenter [121].

The ultimate length scale for mechanical properties measurements is the few-atom scale, which is clearly outside the main scope of this chapter, but may be a source of insight into the behavior of practical materials, and may also be important in establishing the accuracy of atomistic modeling approaches such as molecular dynamics. In this regard, the results reported by Rubio-Bollinger et al. [122], which seem to show that a chain of gold atoms can have a strength value (calculated by the authors from the results in [122])

surpassing that of high-strength steel, stand as a challenge to material testers and material developers alike.

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